GR-CPCI-GR740

Development Board

User's Manual

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1 Introduction

1.1 Scope of the Document

This document establishes the User's Manual for the development board GR-CPCI-GR740.

Information in this document applies to GR-CPCI-GR740 Revision 1.2 or later. Please contact support@gaisler.com for technical questions and for document versions applicable to earlier board revisions.

Please see https://www.gaisler.com/products/gr-cpci-gr740 for the latest available resources for the development board.

1.2 Reference Documents

[RD1] "Quad Core LEON4 SPARC V8 Processor, GR740, Data Sheet and User's Manual",Frontgrade Gaisler, GR740-UM-DS, available from http://www.gaisler.com/gr740

[RD2] GR-CPCI-GR740_schematic.pdf, Schematic; part of GR-CPCI-GR740 Documentation Archive(GR740_20180818.zip) available on https://www.gaisler.com/products/gr-cpci-gr740

[RD3] GR-CPCI-GR740_assy_drawing.pdf, Assembly Drawing; part of GR-CPCI-GR740 Documentation Archive(GR740_20190213.zip) available on https://www.gaisler.com/products/gr-cpci-gr740

[RD4] GRMON3 User Manual, https://www.gaisler.com/GRMON3

[RD5] GR-MEZZ Technical Note, Technical Note about Mezzanine connectors

2 Abbreviations

ASIC	Application Specific Integrated Circuit.
CPCI	Compact Peripheral Connect Interface
DIL	Dual In-Line
DSU	Debug Support Unit
ESD	Electro-Static Discharge
FP	Front Panel
GMII	Gigibit Media Independent Interface
GPIO	General Purpose Input / Output
I/O	Input/Output
IP	Intellectual Property
LA	Logic Analyser
MII	Media Independent Interface
MUX	Multiplexer
PCB	Printed Circuit Board
SOC	System On a Chip
SPW	Spacewire
TBD	To Be Defined

3 Introduction

3.1 Overview

This document describes the *GR-CPCI-GR740* Development Board.

This equipment is intended to be used for the functional validation of the *Frontgrade Gaisler GR740 Processor*. Furthermore, this board provides developers with a convenient hardware platform for the evaluation and development of software for the *GR740* processor.

The *GR740* processor is a radiation-hard system-on-a-chip featuring a quad-core fault-tolerant *LEON4 SPARC* V8 processor, with an 8-port SpaceWire router, PCI initiator/target interface, CAN 2.0 interfaces and 10/100/1000 Mbit Ethernet interfaces. This device is further described in [RD1].

The *GR-CPCI-GR740* Development Board comprises a custom designed PCB in a 6U Compact PCI format, making the board suitable for stand-alone bench top development, or if required, to be mounted in a 6U CPCI Rack, or in a bench-top enclosure.

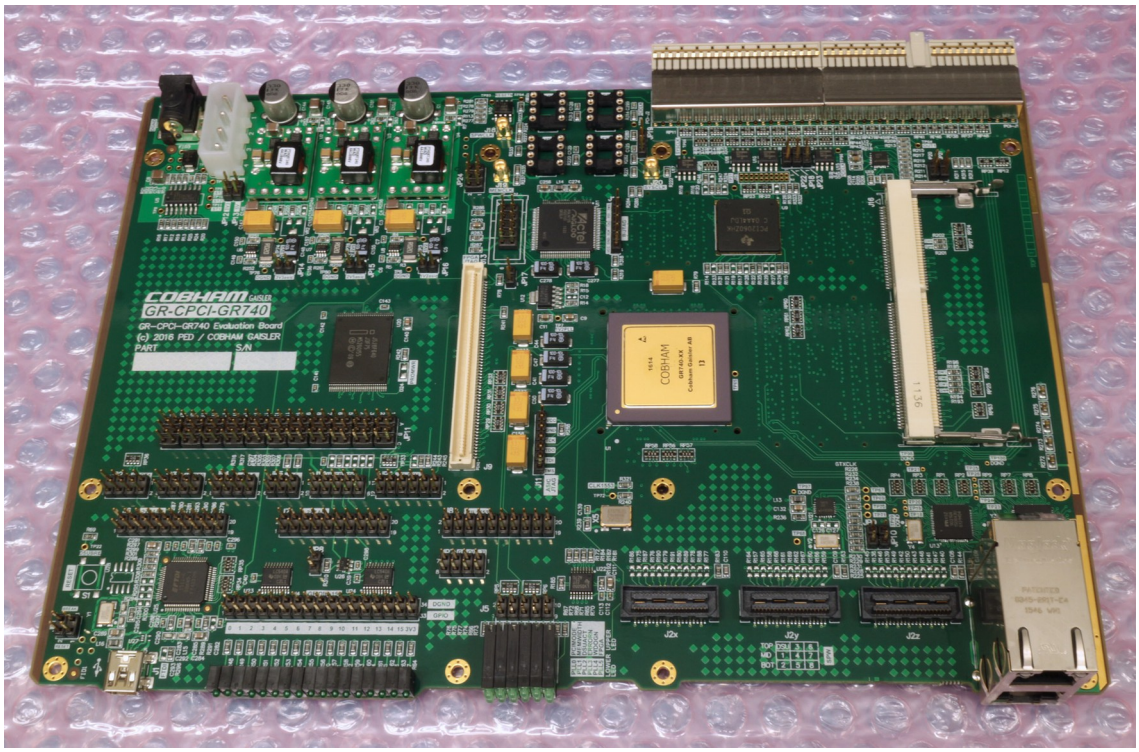


Figure 3-1: GR-CPCI-GR740 Development Board

The principle interfaces and functions are accessible on the front and back edges of the board, and secondary interfaces via headers on the board.

The board contains the following main items as detailed in section of this document:

- GR740 Processor, in PBGA625 package. Note: There have been variants of the board manufactured with a socket or with the GR740 in ceramic package. Figure 3-1 shows the board with a CLGA625.
- CPCI Interface (32 bit) configurable with jumpers for Host or Peripheral operation
- PCI arbiter implemented in a separate FPGA
- Memory
  - SDRAM Configurable 48/96 bits wide, PC133-SODIMM
  - Parallel Boot flash64 Mbit (16bit wide x 4M or 8bit wide x 8M)
  - Memory expansion connector for interface to external devices (16 bit wide Data)
- Power, Reset, Clock and Auxiliary circuits
- Interface circuits required for the features listed below

The interface connectors on the Front edge of the board provide:

- Dual RJ45 10/100/1000 Mbit GMII/MII Ethernet interface (KSZ9021GN)
- 8 port SPW interface (8 x MDM9S) – with LVDS re-driver circuits as buffer to external signals
- SPW Debug Comm. Link (MDM9S)
- 16 bit General Purpose I/O (34 pin 0.1” ribbon cable style connector)
- FTDI Serial to USB interface (FT4232HL with USB-Mini-AB)

The interface connectors on the Back edge of the board provide:

- Compact PCI interface (32 bit, 33/66MHz), configurable for Host or Peripheral slot
- Input power connector : +5V nom. (Range 4.5V to 14.5V)

To enable convenient connection to the interfaces, most connector types and pin-outs are compatible with the standard connector types for these types of interfaces.

Additionally, on-board headers and components provide access to the following functions/ features:

- DIP switches for GPIO signal configuration
- LED indicators connected to GPIO signals
- DIP Switch for Bootstrap and PLL interface configuration
- SPI interface user connections on 0.1” header
- JTAG Debug interface
- 4 pin IDE style power connector
- Push Button switch for RESET and toggle switch (on/off) for BREAK
- LED indicators for POWER, ERRORN, DSU Active and GPIO

- Assorted jumpers and Test Points for configuration and Test of the board

Furthermore, to accommodate the optional/alternative I/O interfaces an accessory board provides

- Dual MIL-1553 Interface (Transceiver/Transformer and D-sub 9 Male connector)
- Dual CAN Interface (CAN Transceivers and two D-sub 9 Male connectors)
- Two Serial UART (RS232 transceivers and two D-sub 9 female connectors)
- 10 pin 0.1” Header for SPI interface

Debug interface support is demonstrated on the board with support for debugging via the following interfaces:

- JTAG
- ETH (EDCL)
- SPW (SPW-DCL)

3.2 Handling

ATTENTION : OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES

This equipment includes SpaceWire (SPW) ports that use Low Voltage Differential Signalling (LVDS), which provides limited common-mode voltage protection. To avoid damage to the SPW interfaces due to excessive common-mode voltage, the following precautions must be observed before powering on any interconnected equipment.

Before connecting any SpaceWire cables, ensure that there is no voltage difference between the grounds of the equipment to be connected. Measure the voltage between the equipment grounds using a voltmeter; the result should be close to 0 V.

After connecting the SpaceWire cables, ensure that the equipment grounds are low-ohmic connected to each other. Measure the resistance between the equipment grounds with a multimeter in resistance mode; the result should be less than 1 Ω.

The SpaceWire standard specifies that the cable-side outer shield is bonded to the connector shell, but it does not define the grounding or bonding of the equipment-side connector shell. Therefore, it cannot be assumed that the different equipment grounds are interconnected solely through the SpaceWire cable.

In this equipment, the SPW connector shells are, by default, bonded to the front panel or local chassis. The chassis is connected to the local SPW circuit ground through a bead.

Users connecting this board to other equipment only via SpaceWire must ensure that the connector shell on the other equipment is also connected to the SPW circuit ground at that end of the interface. If this is not the case, grounding must be provided by other means (e.g., a dedicated grounding wire).

For the GR-CPCI-GR740 Development Board, version 1.1 and earlier, the SPW interfaces do not support cold sparing during power-up or shutdown.

All SPW input signals must therefore remain in an undriven state during board startup and shutdown.

For later versions of this equipment, the SPW interfaces support cold sparing during both power-up and shutdown.

4 Board Design

4.1 GR740 Processor

The *Frontgrade Gaisler GR740 processor* is a radiation-hard system-on-a-chip featuring a quad-core fault-tolerant *LEON4 SPARC* V8 processor, and a set of IP cores connected through AMBA AHB/APB buses as represented in the figure below and as specified in [RD1].

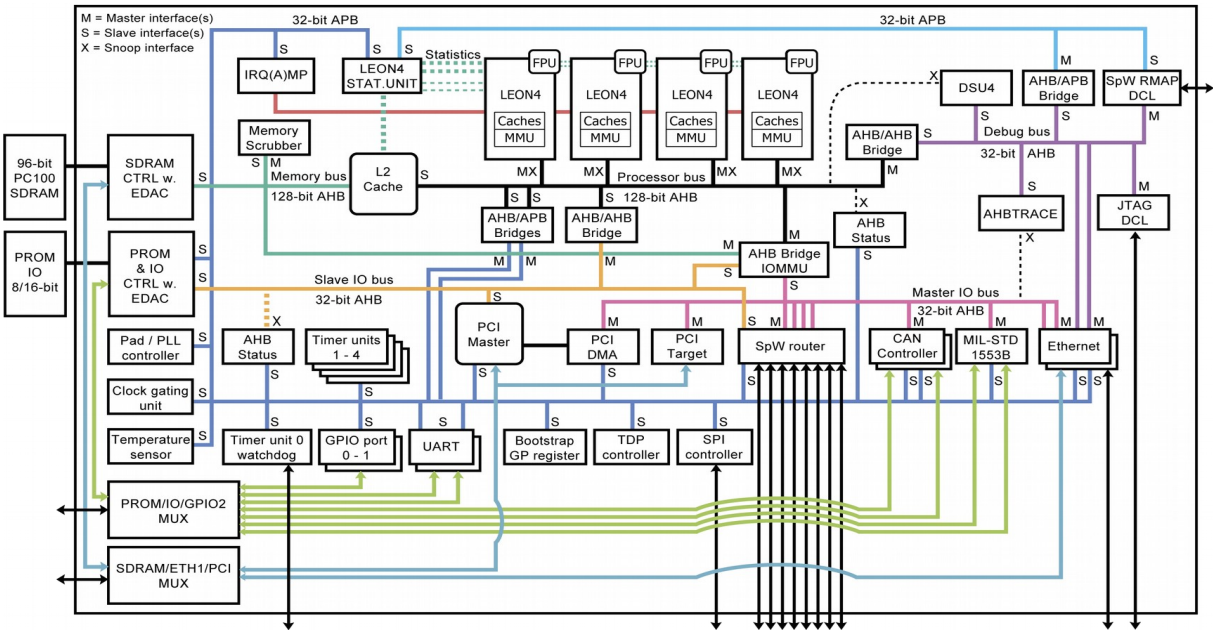


Figure 4-1: GR740 SOC Block Diagram

The device is available in CCGA625, CLGA625 and PBGA625 package type, that are functionally identical. Device packaging dimensions and details are available in [RD1] section 40.4.

Figure 4-2: GR740 Package

The details of the interfaces, operation and programming of the GR740 processor are given in [RD1].

4.2 Board Block Diagram

The *GR-CPCI-GR740* Board provides the electrical functions and interfaces as represented in the block diagram, Figure 4-4.

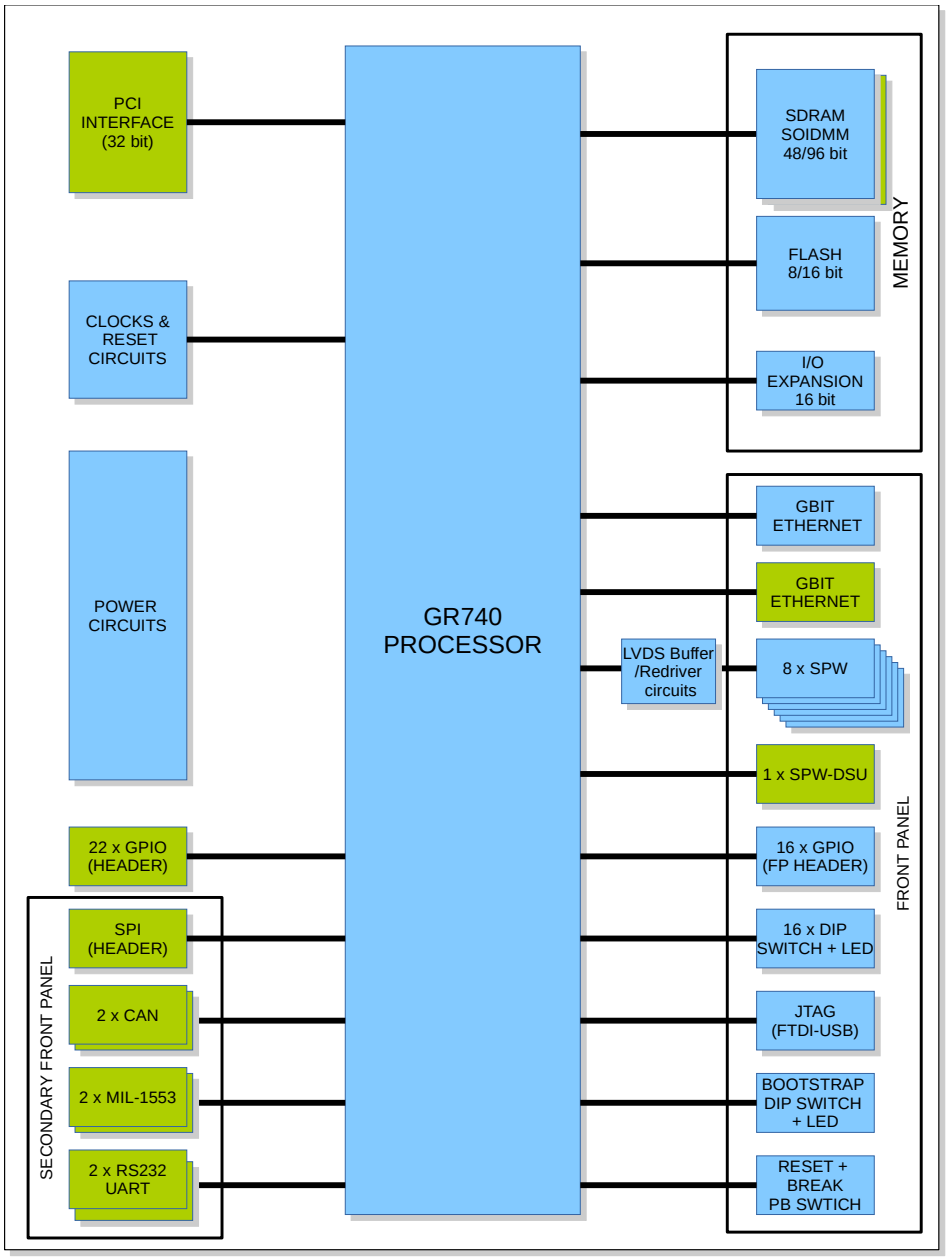


Figure 4-3: GR-CPCI-GR740 Board Block Diagram

Note that not all features and interface are available at the same time, and the

configuration of jumpers and connectors plus some programming of registers is required to access some of the features. The configurable/optional features are marked light-green in the figure above.

4.3 Board Mechanical Configuration

The Main PCB is a 6U Compact PCI format board (233.5 x 160mm) and can be used 'stand-alone' on the bench-top simply using an external +5V power supply, or can be plugged in to a Compact PCI backplane.

Figure 3-1, shows the board as a stand alone PCB. However, for installation into a Compact PCI rack, this board is provided with a custom CPCI front panel with the appropriate connector cut-outs. The board in the standard configuration with the with CPCI front panel mounted is shown in Figure 4-4.

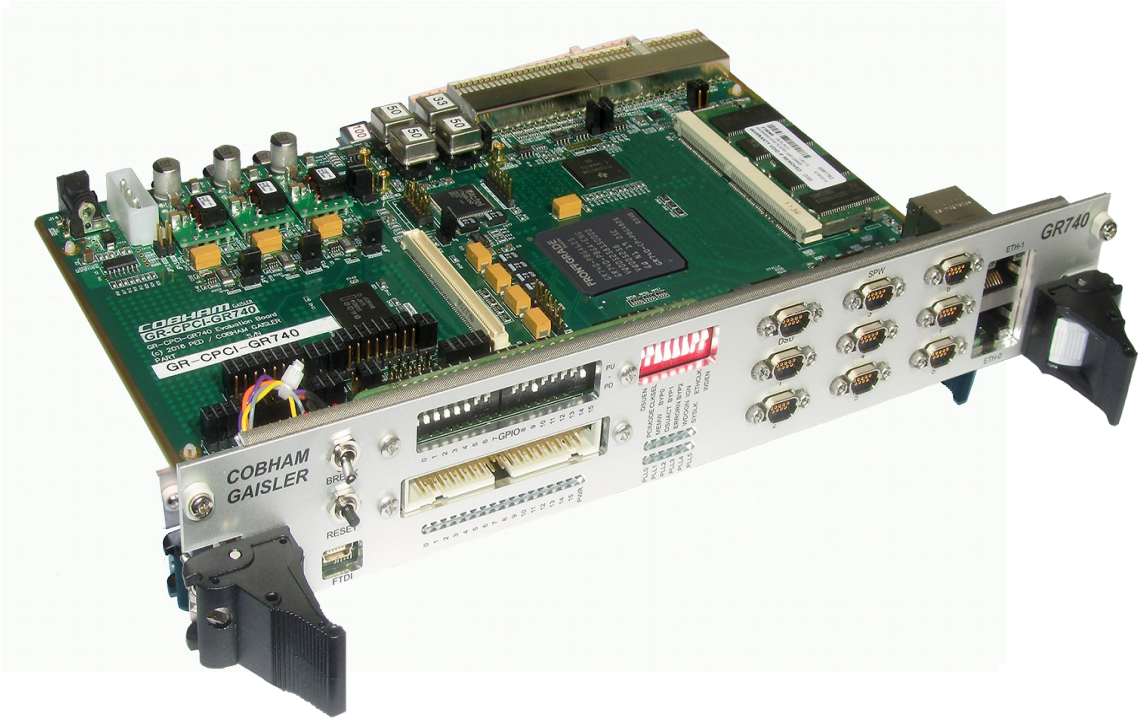


Figure 4-4: GR-CPCI-GR740 Board with CPCI Front Panel

As an alternative to the Compact PCI 6U format of the board, this concept allows the same PCB design to be installed in a Elma Type 33 style case to allow convenient bench-top use of the Unit, in a similar manner to other Frontgrade Gaisler development boards (Figure 4-5).

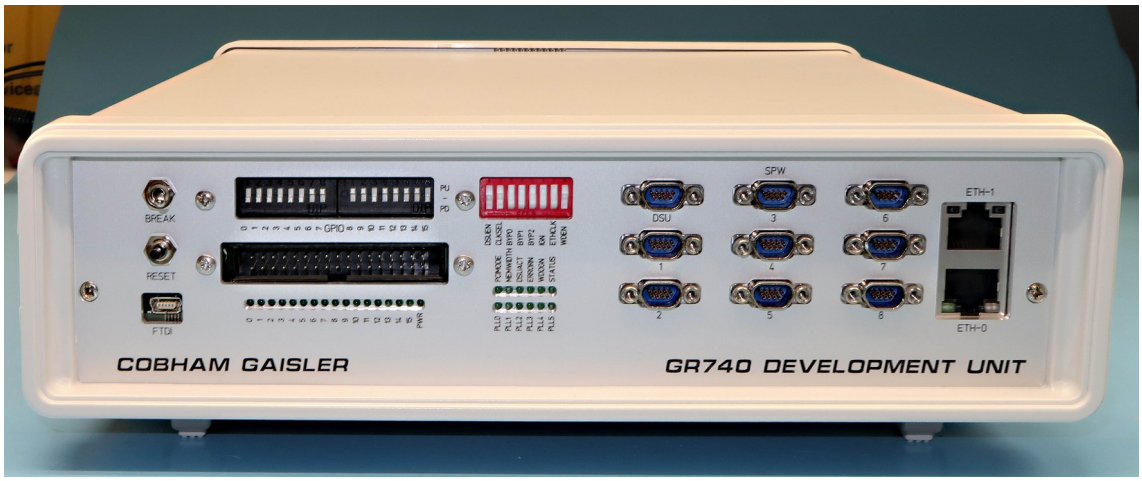


Figure 4-5: GR-GR740-BOX Bench-top Unit

4.4 Front Panel

The front panel of the *GR-CPCI-GR740* Board is conceived as shown in Figure 4-6.

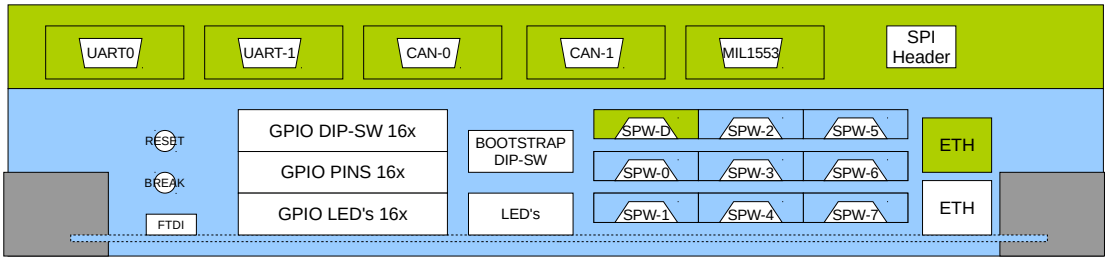


Figure 4-6: GR-CPCI-GR740 board Front Panel Concept

The main front panel of the device contains the connectors, switches and LED's for the main functions of the board. Additionally, on this panel the second Ethernet and the Spacewire-DSU connector are included. This panel is a standard 6U x 2 slot wide panel. A small PCB is required behind the front panel to be able to mount and support the GPIO switches and connector (Figure 4-7). A second optional 1 Slot wide front panel connects to a custom accessory board and provides standard connector interfaces for UART (RS232) MIL-1553, CAN and SPI interfaces.

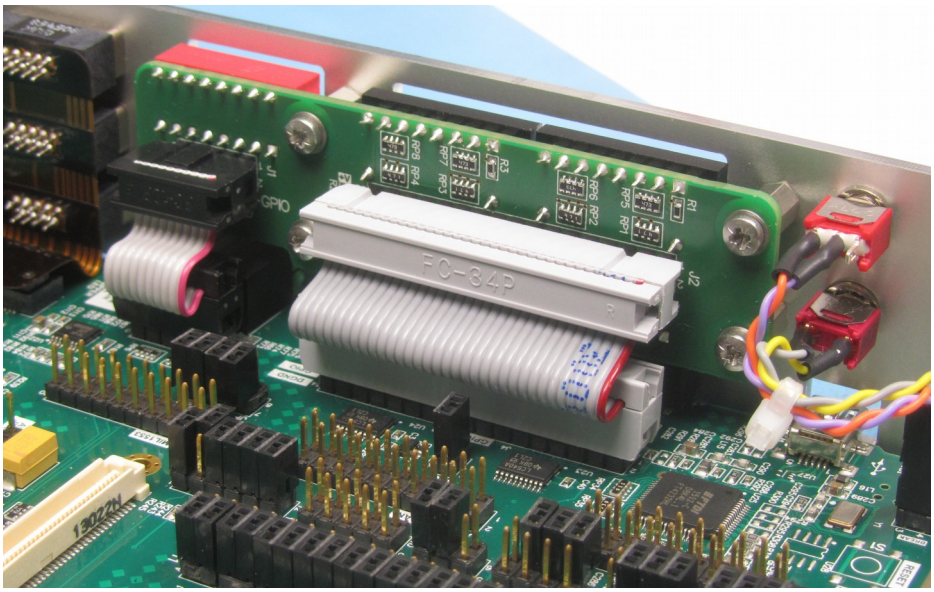


Figure 4-7: Auxiliary PCB for DIP Switches and front panel GPIO connections

If the board is to be housed in an enclosure, then this same front-panel layout is transferred to the ELMA 33 series front panel layout.

The optional/alternative interfaces are mounted on a separate PCB, as an optional accessory board, which will require an additional slot in the 6U rack design.

In the enclosure version of the board, since there is not enough front-panel height available to fit these connectors, this accessory PCB is mounted at the back of the enclosure, and the ribbon cable appropriately adapted.

4.5 Memory

The memory configuration installed on the board comprises:

- SODIMM socket for SODIMM mounted SDRAM
- 64 Mbit of flash PROM, in Parallel 8/16 bit flash device

4.5.1 SDRAM Memory Interface configuration

The *GR-CPCI-GR740* board provides a 96 bit wide SDRAM data interface using two SODIMM modules.

However, the *GR740* processor has various memory operation modes which includes both full-width (96 bit data) and half-width (48 bit data) operation, and the data/control bits for the upper 48 data bits of the SDRAM interface are multi-functional pins shared with the PCI and/or Ethernet_1 interfaces.

In order to accommodate this the *GR-CPCI-GR740* board implements a simple scheme where one of three bridging plugs is to be installed as represented in Figure 4-8.

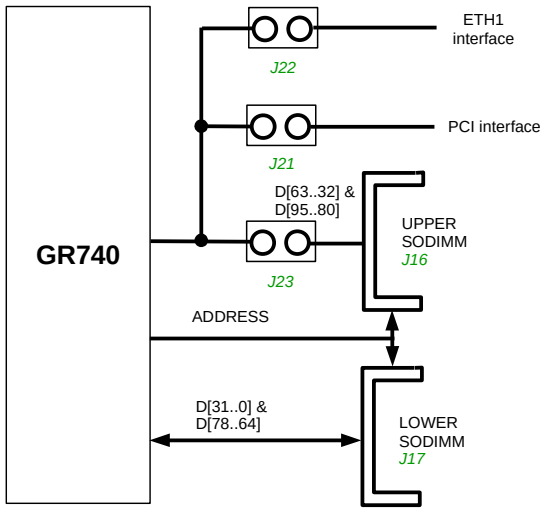


Figure 4-8: Configuration plugs for 48/96 bit SDRAM memory

Install plug on J21 => 48 bit memory + PCI

Install plug on J22 => 48 bit memory + ETH1

Install plug on J23 => 96 bit memory

Figure 4-9 shows the location of the connectors J21, J22, J23 on the bottom side of the PCB.

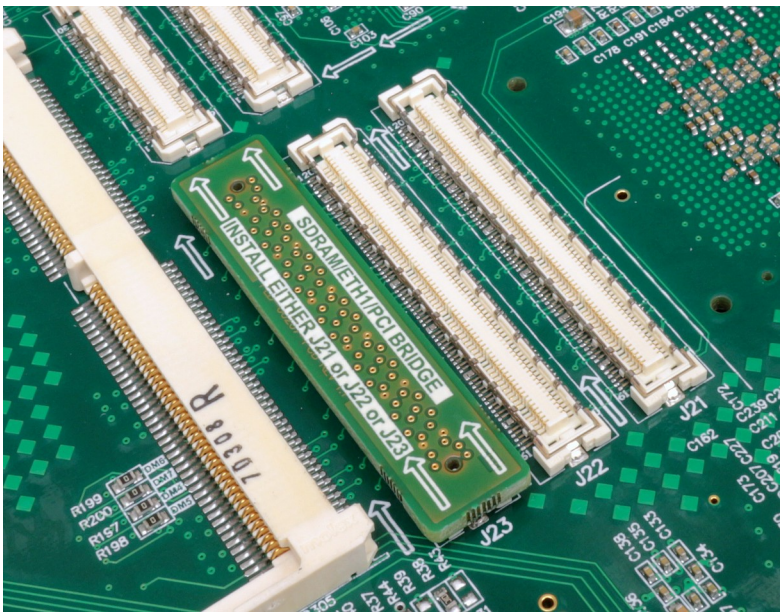


Figure 4-9: Configuration plugs installation on bottom side of PCB

Note: When the Plug-on board is connected, the *PCI-MODE* and *MEMWIDTH* signals are automatically strapped high/low as appropriate. The state of the *PCI-MODE* and *MEMWIDTH* signals is indicated by front-panel LED's.

4.5.2 SDRAM SODIMM 48/96 Bit Interface

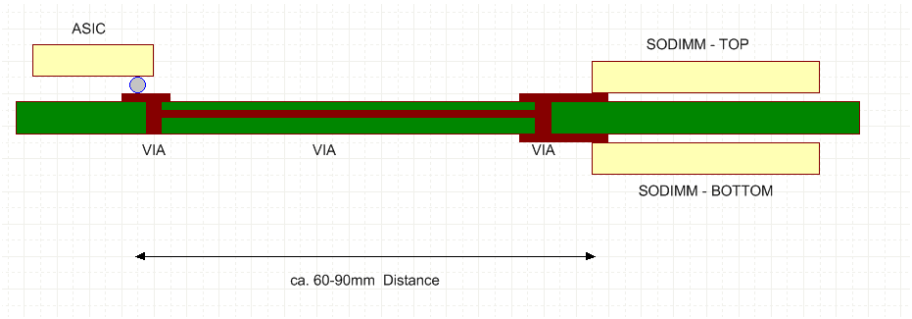
The GR740 processor incorporates a 96 bit wide PC-100 SDRAM Data interface (64 bits data plus 32 bits EDAC check bits).

To accommodate this in a flexible way, two 144 pin SDRAM SODIMM sockets are implemented on board, one socket for the 48 bit memory configuration (lower 32 bits data plus its corresponding 16 EDAC check bits), a second socket for the upper 32 data bits plus its corresponding 16 EDAC check bit used in the 96 bit memory configuration.

If 48 bit memory interface is selected, an SODIMM module should be installed in the upper SODIMM socket (*J16).*

If 96 bit memory interface is selected, then an SODIMM module should be installed in the each of the SODIMM sockets (*J16 & J17*).

Due to the size and configuration of the SODIMM sockets, one socket is mounted on the top side and the other socket on the bottom side of the board, in a 'mirror image' as represented in the figure below.



Note that the height of the SODIMM socket on the bottom side of the board is approximately 5.2mm. Strictly speaking, the CPCI specification only allows an envelope of 2.54mm for the component heights on the bottom side of the board, and the board is therefore not fully compliant. This is unlikely to cause an actual problem in use, since the volume required by the bottom side socket is most likely to be 'free air' in any normal single or dual slot board mounted in the adjacent slot. However, it is necessary to take care when installing and removing the card from a PCI rack. Do not simply yank the card out of the rack since this bottom side SODIMM socket will make contact against the front panel of the adjacent card when you try to slide it out of the rack, and this may damage the board. YOU MUST NOT TRY TO USE FORCE TO REMOVE THE CARD! Instead the adjacent card will have to be loosened or removed first in order to allow the GR-CPCI-GR740 card to be removed.

SDRAM Clock Phase Adjustment

A clock phase shifter circuit is defined to enable an adjustable phase shift of the SD_CLK phase relation between ASIC and SODIMM module to be performed.

A programmable clock generator circuit based on the IDT Versa clock device *5P49V5943* (or a similar one) is implemented.

This is a flexible device which is controlled via an I2C interface. The automatic programming of the device requires that an I2C sequencer and parameter storage which is implemented in the on-board FPGA.

4.5.3 PROMIO / Interface configuration

For the multiplexed PROMIO signals, the GR740 and board supports two base options:

1. Full PROM/IO mode. Set GPIO[15] low and set all JP11 jumpers to the A-B position, connect JP6 jumpers and disconnect the peripheral mezzanine from the board.
2. All peripheral mode. Set GPIO[15] high and set all JP11 jumpers to the C-D position, disconnect JP6 jumpers and connect the peripheral mezzanine.

Note: It is possible to also create custom configurations in between these two extremes by starting with the GR740 in one of these two modes and then reprogram the pin multiplexing in software during start-up through the GR740's register interface. To

support this type of usage, the board has individual jumpers in JP11 (as shown in Table 1), JP6 and JP7. When doing this, the user must take into account that some pins are configured in the opposite state before it has been reprogrammed, and avoid possible output collisions and logical errors.

JP11 jumper	Pin configuration at position A-B	Pin configuration at position C-D
1	PROMIO_ADDR27	UART_TXD0
2	PROMIO_ADDR26	UART_TXD1
3	PROMIO_ADDR25	1553TXA
4	PROMIO_ADDR24	1553TXNA
5	PROMIO_ADDR23	1553RXENA
6	PROMIO_ADDR22	1553TXB
7	PROMIO_ADDR21	1553TXNB
8	PROMIO_ADDR20	1553RXENB
9	PROMIO_ADDR19	SPWDCL_DBG_TXD
10	PROMIO_ADDR18	SPWDCL_DBG_TXS
11	PROMIO_ADDR17	UART_RTSN0
12	PROMIO_ADDR16	UART_RTSN1
13	PROMIO_DATA7	UART_RXD0
14	PROMIO_DATA6	UART_RXD1
15	PROMIO_DATA5	CAN_RX0
16	PROMIO_DATA4	CAN_RX1
17	PROMIO_DATA3	1553RXA
18	PROMIO_DATA2	1553RXNA
19	PROMIO_DATA1	1553RXB
20	PROMIO_DATA0	1553RXNB
21	PROMIO_CEN1	CAN_TX0
22	PROMIO_IOSN	CAN_TX1

Table 1: JP11 individual jumper configuration

Note: Revision 1.0 and revision 1.1 of the PCB have a limitation with floating address lines. If for instance, we use all 1553 pins, which means that 1553 signals on the board (JP11 7 and 8) have to be connected to the GR740 pins instead of PROMIO_ADDR 21 and 20. This will leave PROMIO_ADDR 21 and 20 floating, which are connected to the flash address inputs 21 and 20. In rev 1.2 of the board, pull-down resistors have been added to ensure that unconnected address lines remain at '0'.

4.5.4 PROMIO / Parallel Flash

This device can be used for Program storage or as a boot device for the board.

This device (Intel/Numonyx/Micron JS28F640J3 Strataflash) provides 64Mbit of Non-Volatile storage, organised as 8M x 8 bits (4M x 16 bits), operating with an I/O voltage

of in the range of 2.7V to +3.3V.

This device is connected to the following *PROMIO* pins:

ADDR[24..0]
DATA[15..8] or [15..0]
OEN
WRITEN
CEN0

The J3 series flash devices can be configured for either 8 or 16 bit operation, by means of a jumper on the board (*JP6 pins 11-12). Note:* if the PROM width is changed via *JP6 pins 11-12* then *GPIO[10]* should also be set to reflect the correct PROM width.

Programming of these flash chips can be performed using the *GRMON3* debug software.

Note: In order to support both 16-bit and 8-bit mode, GR740.DATA[7:0] is connected to the Flash device's DQ[15:8] and GR740.DATA[15:8] is connected to the Flash device's DQ[7:0]. This means that CFI read data and commands need to be byte-swapped in 16-bit mode. The GRMON3 debug monitor does this automatically but this needs to be taken into account for Flash routines implemented in software running on the GR740.

To allow the User to prevent the contents of the flash memory from being overwritten under software control, the Write-Protect pin can be tied to *DGND* by installing the jumper *JP6 pin 1-2*.

Under certain circumstances, it may be desirable to inhibit the operation of the Flash PROM (e.g. if system booting and program loading via Spacewire RMAP protocol is required instead, or if an external MRAM/PROM is installed on the memory expansion connector, or if the *PROMIO* pins are to be used for their alternate Interface functions). To facilitate this, a Jumper *JP6 pin 3-4* is provided which connects/disconnects the *ROMSN0* pin of the *GR740* to the Chip Enable pin of the flash Prom. In normal operation, to boot from this flash prom, the jumper (*JP6 pin 3-4*) should be installed. To inhibit the operation of the flash prom, the jumper should be removed.

4.5.5 Memory Expansion

The GR740 processor does not support the addition of SRAM memory.

However, the following memory bus signals are connected to a 120 pin AMP connector (AMP 5-177984-5), *J9*:

DATA[15..0]
ADDR[27..0]
WRITEN
READ
OEN
IOSN

CEN[1..0]
BRDYN
EXP_CLK
RESETN

This connector and these signals makes it feasible for users to define peripherals mapped in the processor I/O space and to implement mezzanine boards which could be connected to this Development Board in a similar manner to the other GR Development Boards.

Note: The pins ADDR[27..16] and DATA[7..0], CEN1 and IOSN can have alternative pin functions depending how the internal registers of the GR740 and board is configured. The signals which are present on this connector will therefore depend on how these pins of the GR740 are configured.

Note: The EXP_CLK signal can be used to provide a Clock to circuits on the Mezzanine. Depending on the configuration required, this connector pin can be connected to either the MEM_EXTCLK or SD_CLK with a zero-ohm resistor soldered to the board to either R246 (default) or R247.

Figure 4-10 shows the pin numbering scheme as implemented on the expansion connector.

Please note that this pin ordering on this connector does not match exactly the pin ordering which you will find on the Tyco part datasheets for the Mezzanine board mating connectors. The reason for this is explained in more detail in the Technical Note, [RD5].

Therefore please take care when designing your own mezzanine boards to take account of this pin ordering.

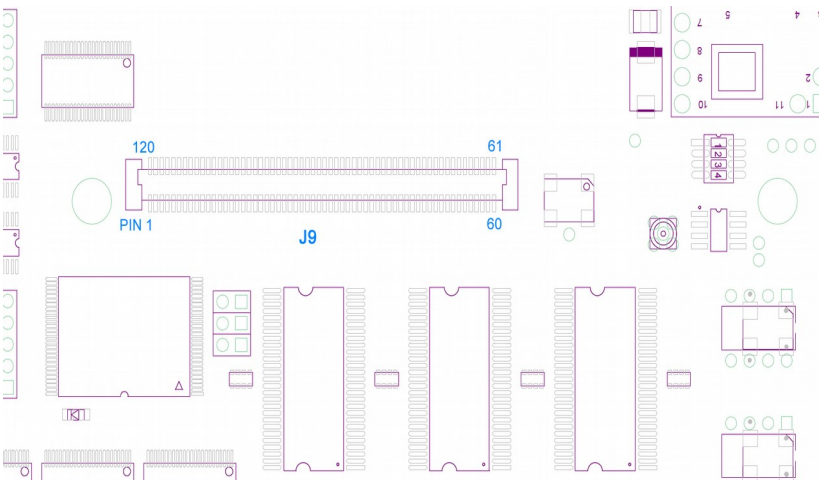


Figure 4-10: Mezzanine Connector Pin Number Ordering

If there is any confusion, or you have any doubts, please do not hesitate to contact support@gaisler.com. Additional dimensional data or Gerber layout information can be provided, if required to aid in the layout of the User's mezzanine board.

4.6 PCI Interface

The *GR740 processor* incorporates a 33MHz/66MHz/32 bit interface and is capable of being configured to be installed in either the SYSTEM slot (HOST) or in PERIPHERAL slots (GUEST).

In order to ensure a compliant PCI signal drive on the CPCI backplane, the *GR740 processor* will require a PCI-PCI bridge circuit on board acting between the *GR740* and the Backplane.

The PCI-PCI Bridge is the Texas Instruments, PCI2060, which fully Supports PCI Local Bus Specification Revision 2.3 and PCI-to-PCI Bridge Specification, Revision 1.1. and is attractive due to its easy availability.

There is also a desire to also be able to test the operation of the *GR740 processor with* direct connection to the backplane. Therefore 4 configurations are to be supported with this board, as represented conceptually in Figure 4-11:

1. GR740 as Host connected to primary side of PCI-PCI Bridge and from there to Backplane
2. GR740 as Peripheral to secondary side of PCI-PCI Bridge and from there to Backplane
3. GR740 as Host connected directly to Backplane
4. GR740 as Peripheral connected directly to Backplane

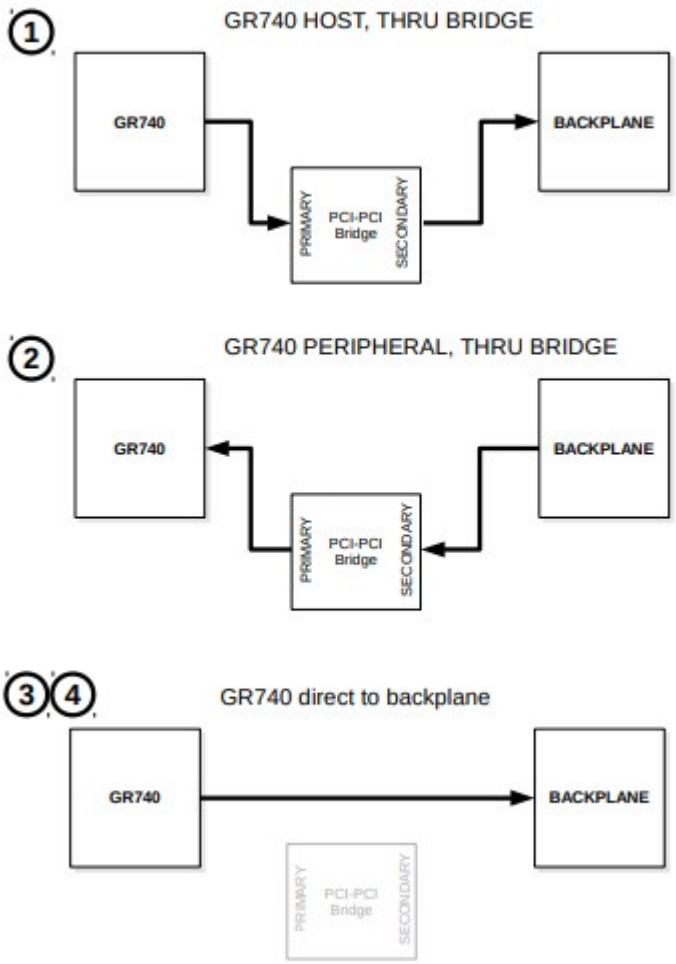


Figure 4-11: PCI Interface Configurations

These multiple configurations create rather a problem for a 'clean' implementation since a method has to be implemented to connect/disconnect and re-arrange the PCI interface signals so that all these configuration can be accommodated.

The solution is represented in block diagram form in Figure 4-12. Four sets of signals are identified: PCI-X (*J42*-Processor), PCI-Y (*J27*-backplane), PCI-P (*J25*-Bridge primary Side) and PCI-S (*J26*-Bridge Secondary side). Different plug-on PCB's are necessary to appropriately connect these sets of signals. These PCB's are simple, without additional active components (only a few pull-up/pull-down resistors). There exists the possibility that these PCB's can conveniently provide measurement/LA test-points for the PCI signals which could be an advantage.

The plug-on board mounts on the bottom side of the PCB in order to provide the most convenient signal routing and layout (Figure 4-14). Note: These mezzanine connectors are not 'keyed', although there is a visual hint whereby the pin 1 of the connectors is

marked by the diagonal corner. Ensure that the PCI-PCI Mezzanine is fitted as shown in Figure 4-13.

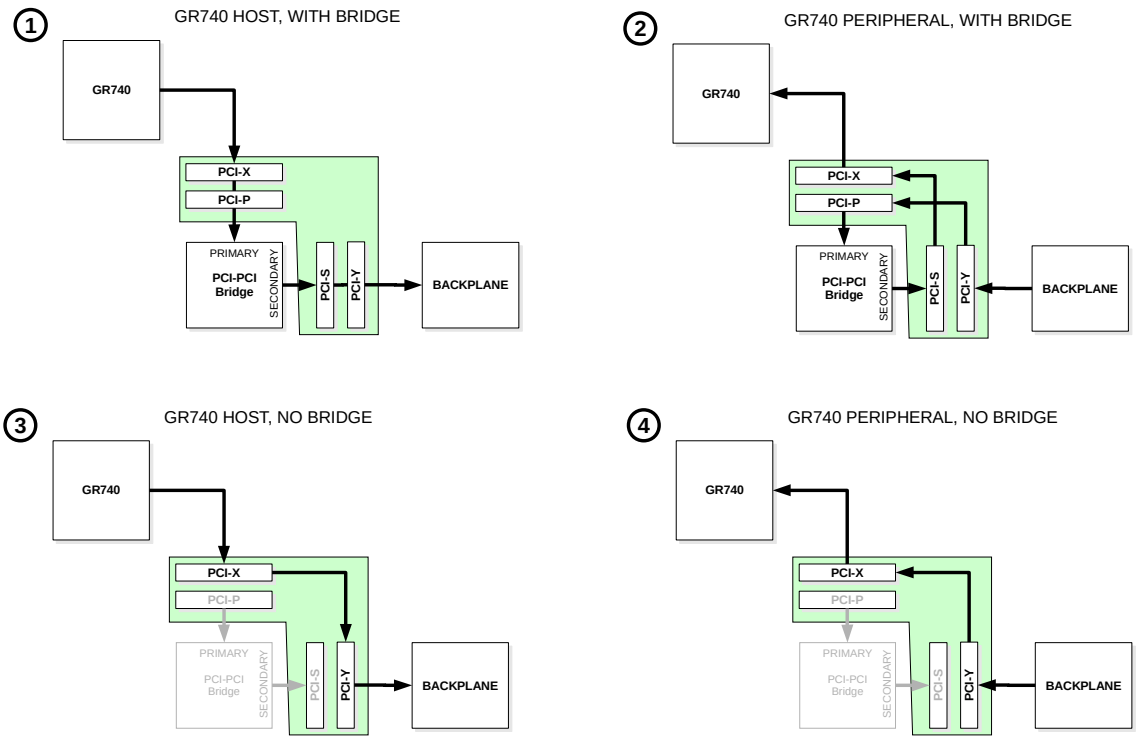


Figure 4-12: PCI Peripheral-Host-Bridge Connections

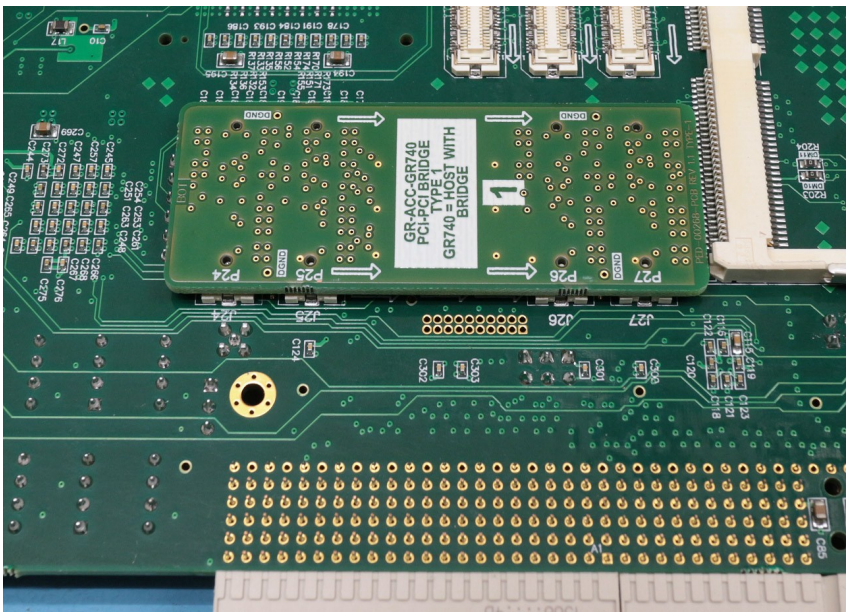


Figure 4-13: PCI-PCI Configuration Mezzanine Mounted – Note the orientation

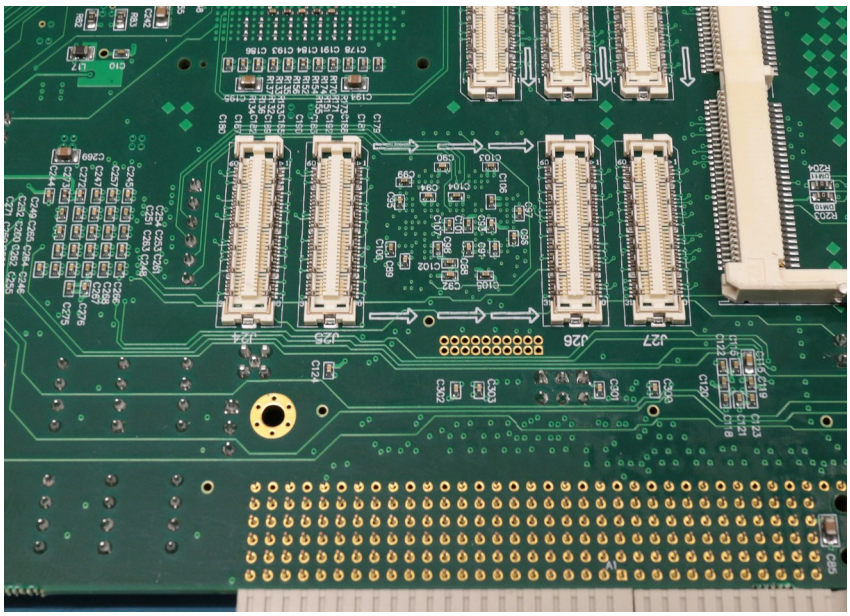


Figure 4-14: Connectors for mounting PCI-PCI Configuration Mezzanine

Note: for strict compliance to CPCI a maximum signal distance from Backplane to Device of 63.5mm (2.5 inch) is specified. This is not be met in all situations.

To provide more explanation, four different aspects are considered:

1. PCI data/address/control bus
2. PCI Clock generation and distribution

3. PCI arbiter interface
4. PCI IDSEL, Reset configuration

4.6.1 PCI data/address/control bus

The signals comprise the data, address and control signals for a 32 bit PCI interface:

PCI_AD[31..0]
PCI_CBE[3..0]
PCI_CLK
PCI_DEVSELN
PCI_FRAMEN
PCI_GNT
PCI_IDSEL
PCI_IRDYN
PCI_PAR
PCI_PERRN
PCI_REQ
PCI_RST
PCI_SERRN
PCI_STOPN
PCI_TRDYN

Note: PCI_LOCKN is not used, and no pin exists on the GR740 for this signal. The primary and secondary side LOCKN signals are pulled to '1' with pull-up resistors on the board.

Note: There is no IDSEL signal interfacing the secondary PCI bus; thus, the entire configuration space of the bridge can only be accessed from the primary bus (this information is from the PCI2060 datasheet).

As shown in Figure 4-12 the schemes for the four supported configurations are:

1. With GR740 as Host with a PCI-PCI Bridge: the GR740 signals connect to Bridge Primary side (X <=> P) and the Backplane signals connect to Bridge Secondary side (S <=> Y)
2. With GR740 as Peripheral with a PCI-PCI Bridge: Backplane signals connect to Bridge Primary side (Y <=> P), GR740 signals connect to Bridge Secondary side (S <=> X)
3. With the GR740 as Host connected directly to Backplane: GR740 signals connect Backplane Connector (X <=> Y); Bridge primary and Secondary signals are not used. The Bridge is switched off (to put all output buffers to Hi-Z) by pulling P_RST low with a jumper.

4. With the GR740 as Peripheral connected directly to Backplane: GR740 signals connect Backplane Connector (X <=> Y); Bridge primary and Secondary signals are not used. Bridge is switched off (to put all output buffers to Hi-Z) by pulling P_RST low with a jumper.

4.6.2 PCI Clock distribution

The various clock distribution schemes for the four supported configurations are shown in block diagram form in Figure 4-15.

1. With GR740 as Host with a PCI-PCI Bridge, a 33/66 MHz oscillator is required, and the zero delay buffer generates 33/66MHz clocks to 3 destinations on the Primary side, to the secondary side clock of the PCI-PCI Bridge and to the 7 slots of the PCI backplane.
2. With GR740 as Peripheral with a PCI-PCI Bridge a 33/66 MHz oscillator is required, and the zero delay buffer generates 33/66MHz clocks to the GR740 and to the secondary side clock of the PCI-PCI Bridge. Additionally, a clock is required for the secondary side arbiter.
3. With the GR740 as Host connected directly to Backplane, a 33/66 MHz oscillator is required, and the zero delay buffer generates 33/66MHz clocks to the GR740 and to the 7 slots of the PCI backplane.
4. With the GR740 as Peripheral connected directly to Backplane, the 33/66 MHz oscillator and zero delay buffer are not required. The PCI_CLK from the backplane connector connects directly to the PCI-CLK input of the GR740.

Notes:

The PCI Bridge chip has the possibility to generate PCI clocks for up to 9 peripherals with nine dedicated output pins on the chip. However, these will not be used and instead three CY2305 Zero Delay buffers are implemented, each with up to 5 outputs.

A feature of the CY2305 circuit is that the outputs can be switched off and put in to Hi-Z, by removing the clock oscillator input to the CY2305. This is necessary in the case that the GR740 is operating as a peripheral with no bridge since the peripheral board should not drive the clocks of the other slots. A jumper JP22 is provided to achieve this.

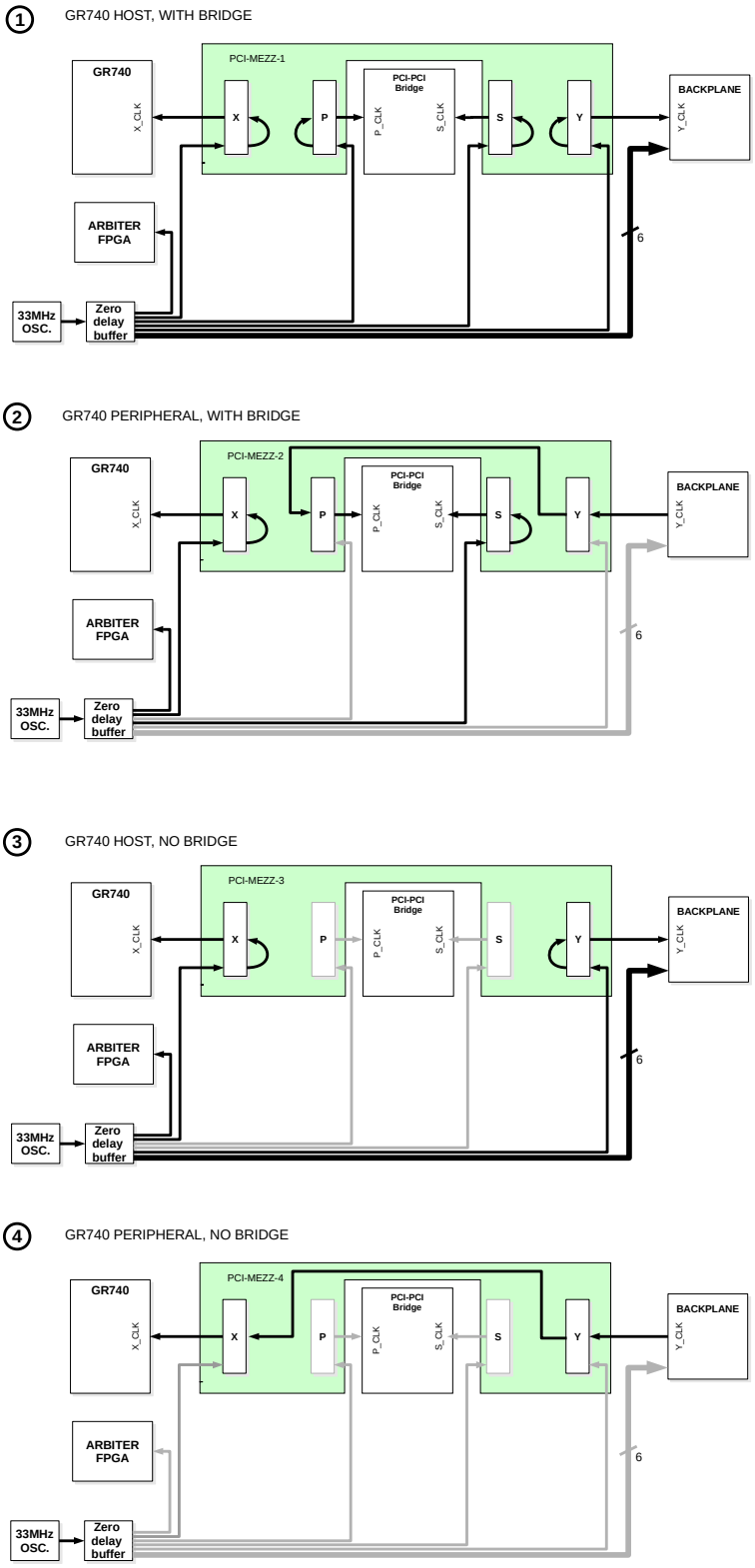


Figure 4-15: PCI Clock Distribution

The PCI Bridge device supports operating modes where the primary and secondary

sides of the bridge are operating at different speeds (either 33 or 66 MHz). It is not immediately clear whether it is necessary to support both Sync/Async clocking 33/66MHz.

4.6.3 Arbiter signal distribution

Arbitration is required in two directions:

1) 8 channels to arbitrate between bridge and the backplane

2) 2 channels to arbitrate between the bridge and the GR740 processor

As represented in Figure 4-16, four situations need to be accommodated:

1. With GR740 as Host with a PCI-PCI Bridge: This requires a 2-master arbiter for the primary bus (GR740,bridge-primary), and an 8-master arbiter for the backplane (bridge-secondary+other boards on backplane).
2. With GR740 as Peripheral with a PCI-PCI Bridge: A two-master arbiter for the secondary bus (GR740,bridge-secondary) is required. The primary side arbitration is handled by the backplane.
3. With the GR740 as Host connected directly to Backplane: An 8 channel Arbiter in the FPGA is connected to the *GR740* and to the other 7 slots of the backplane via the backplane connector.
4. With the GR740 as Peripheral connected directly to Backplane: No arbiter required. The *GNTN* and *REQN* from the backplane are connected to the GR740. The other Arbiter output connections to the backplane from the FPGA are set to high impedance.

Logic for the 8-channel and 2-channel arbiter is implemented in a separate FPGA device (see section 4.8).

Note that, although the PCI-PCI Bridge contains an 8 channel arbiter circuit. this will not be used. The PCI-PCI Bridge Arbiter is switched off by pulling its *S_CFN* pin high. (If the PCI-PCI Bridge Arbiter was to be used, this would make the switch between primary <=> secondary directions very difficult. Instead this can be more simply handled in the FPGA device where by it can reconfigure its directions depending on which of the four modes it is to operate in according to the table below:

Configuration	2-Master Arbiter	8 Master Arbiter
1	GNT/REQ9 & GNT/REQ10	GNT/REQ[6..1] & GNT/REQ[7..8]
2	GNT/REQ8 & GNT/REQ10	not used
3	not used	GNT/REQ[6..1] & GNT/REQ[7] & [10]
4	not used	not used

Table 2: PCI Arbiter connections for modes 1-4

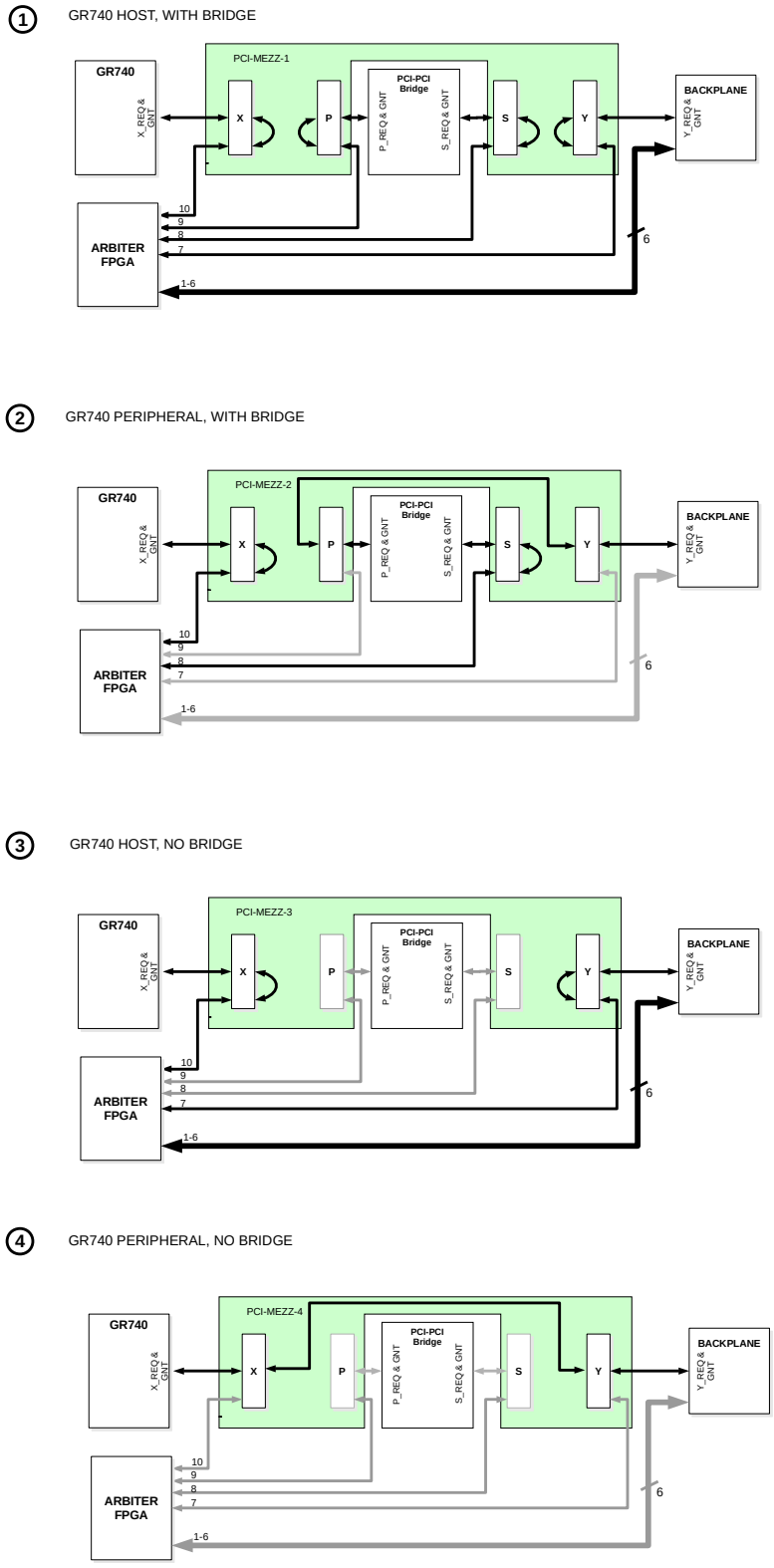


Figure 4-16: Arbiter Signal Distribution

4.6.4 PCI Interrupts & PCI_HOSTN

The *GR740 Processor* has input pins to support up to four PCI interrupts. These are connected directly from the backplane to the *GR740*, and have no involvement of the PCI-Bridge.

4.6.5 PCI_IDSEL

For the IDSEL signal of the PCI interface, the plug-on boards will configure the following four options.

1. With GR740 as Host with a PCI-PCI Bridge: One of the *AD[31..11]* lines is connected to the *P_IDSEL* pin of the PCI-PCI Bridge. *AD[31]* is chosen for this function.
2. With GR740 as Peripheral with a PCI-PCI Bridge: The *Y_IDSEL* from the backplane connects to the *P_IDSEL* on the primary side of the PCI-PCI Bridge. On the secondary of the PCI Bridge, Address line S_AD[31] f is connected to the *X_IDSEL* input of the *GR740*.
3. With the GR740 as Host connected directly to Backplane: There are no connections required since the Host signals the peripherals via the lines *AD[31..16]* which connects to their *IDSEL* inputs according to the arrangement of the backplane. However, The *X_IDSEL* input to the *GR740* is pulled 'low' as a precaution.
4. With the GR740 as Peripheral connected directly to Backplane: the *Y_IDSEL* from the backplane connects directly to the *X_IDSEL* of the *GR740*.

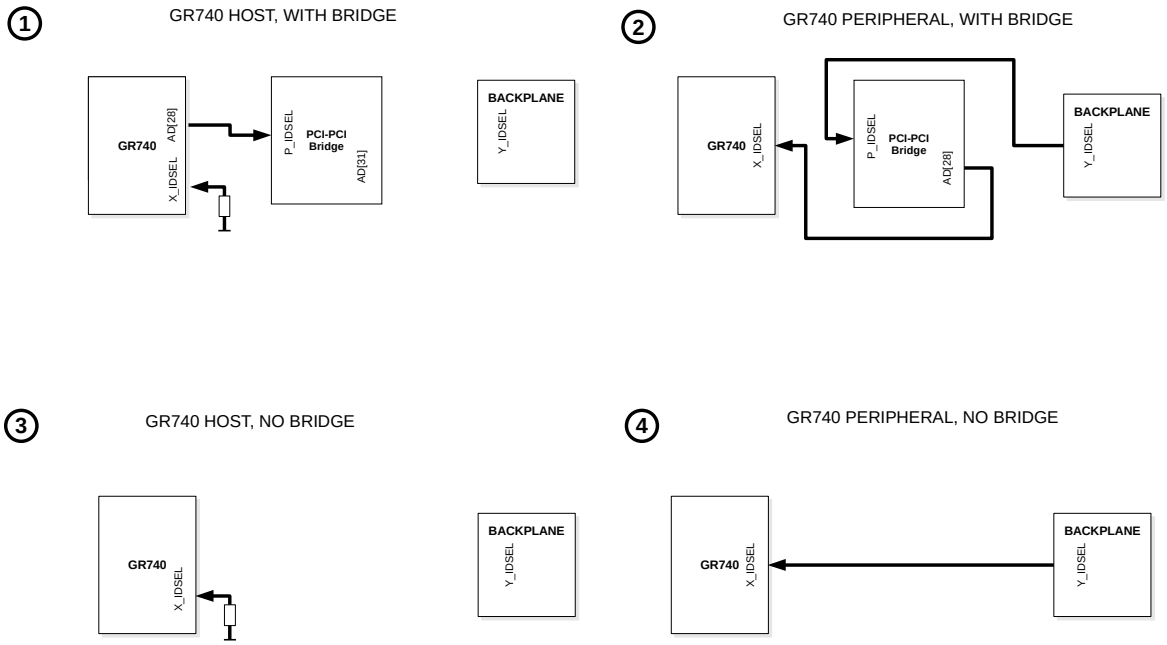


Figure 4-17: IDSEL Distribution

4.6.6 PCI Reset

The PCI controller on the GR740 is reset via the RESETN input that resets the full device. The *GR740* does not have a separate *PCI_RSTN* handling (neither input nor output). The connection to the *PCI_RSTN* of the backplane therefore needs to be handled on the board.

The reset jumper JP19 must be disconnected when using the bridge in host mode. The bridge already takes in RESETN on the primary side and generates PCI_RST on the secondary side, setting JP19 1-2 creates a loop back from PCI_RST into the reset generator and the board never leaves reset.

In peripheral mode, the PCIRST from the backplane is connected to board's reset generator so that a PCI_RSTN input will generate a full reset of the GR740 board.

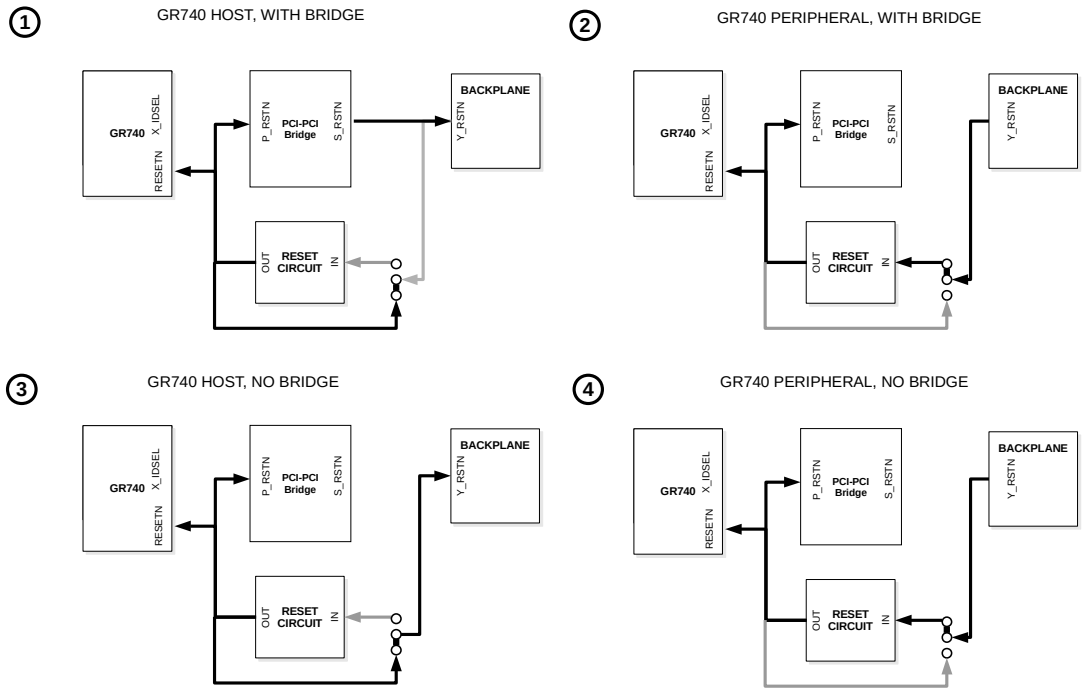


Figure 4-18: PCI_Reset Configuration

4.6.7 33 / 66 MHz PCI Bus Speed

The GR740 ASIC is capable of operating either with a 33 MHz or 66 MHz PCI bus speed. If operating as a Host in the System slot, the GR740 Board is required to provide the PCI Clock to the other slots via the Backplane and an oscillator must be provided on the board (X3). To enable either 33 MHz or 66 MHz to be used, this oscillator is socketed and the user can exchange and install the correct oscillator, as appropriate.

A backplane pin M66EN pin is connected to the ASIC, and is intended in the PCI

specification to signal to the PCI-Host whether the Backplane/System is capable of operating at 66MHz clock frequency. In principle this could be used to automatically select whether a 33MHz or 66MHz clock is used for the PCI interface. However, there is no mechanism on this board to automatically change this frequency, and the User is instead required to install the desired Oscillator in socket X3 in order to use either 33 or 66 MHz as the PCI frequency when in PCI-Host mode. Note also that 66MHz clocking of PCI is in principle only valid for systems with a maximum of 5 slots.

If, in a system capable of 66MHz bus speed, it is for some reason it is required to run the bus at 33MHz, this can be achieved by installing the Jumper *JP23*, which will force the M66EN of the backplane to DGND.

4.7 Ethernet Interface

The GR740 processor device incorporates two Ethernet controllers with support for GMII and MII interfaces, and the GR-CPCI-GR740 Development Board has two Micrel KSZ9021GN 10/100/1000Mbit/s Ethernet PHY transceivers. These are connected to a dual RJ45 connector on board (J3).

For more information on the registers and functionality of the Ethernet MAC+PHY device please refer to the data sheet for the KSZ9021GN device.

The GMII Ethernet PHY's are provided with a 125 MHz clock derived from the oscillator Y2 on the board.

Ethernet Interface 0 has a hard-wire PHY Address of 1 (“001”) on this board.

Ethernet Interface 1 has a hard-wire PHY Address of 2 (“010”) on this board.

Note that, if using the Ethernet interfaces for the EDCL Debug link, it is necessary to appropriately set the GPIO DIP switches at power-up/reset of the board to Boot-strap the following settings:

GPIO[1:0] *(DIP switch FP-S1-1 & -2)* sets the two least significant address bits of the IP and MAC address for Ethernet Debug Communication Link 0 and Link 1

GPIO[3..2] *(DIP switch FP-S1-3 & -4)* sets the bits [3..2] of the least significant address nibble of the IP and MAC address for Ethernet Debug Comm.Link 0.

GPIO[5..4] *(DIP switch FP-S1-5 & -6)* sets the bits [3..2] of the least significant address nibble of the IP and MAC address for Ethernet Debug Comm. Link 1.

GPIO[8] *(DIP switch FP-S2-1)* selects if Ethernet Debug Communication Link 0 traffic should be routed over the Debug AHB bus (HIGH) or the Master I/O AHB bus (LOW).

GPIO[9] *(DIP switch FP-S2-2)* selects if Ethernet Debug Communication Link 1 traffic should be routed over the Debug AHB bus (HIGH) or the Master I/O AHB bus (LOW).

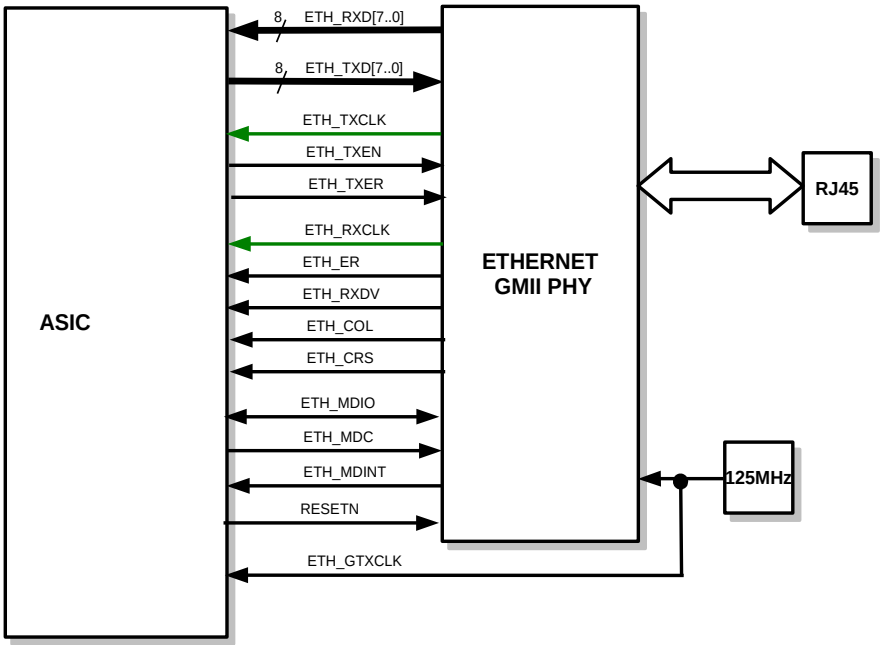


Figure 4-19: Block diagram of Ethernet GMII/MII Interface (one of 2 interfaces shown)

Note:

After reset, the first Ethernet debug communication link will attempt to configure the Ethernet PHY. In order for this to succeed, the Ethernet 0 port must be connected to a switch or other networking equipment. Once the PHY for Ethernet 0 has been configured then control over the shared MDIO bus will be given to Ethernet 1. This means that in order to use the Ethernet 1 debug communication link, Ethernet 0 must also be connected to a network.

GTX Clock Phase Adjustment

A clock phase shifter circuit is defined to enable an adjustable phase shift of the gtx_clk phase relation between phy and ASIC to be performed.

A programmable clock generator circuit based on the IDT Versa clock device *5P49V5943* (or a similar one) is implemented.

This is a flexible device which is controlled via an I2C interface. The automatic programming of the device requires that an I2C sequencer and parameter storage which is implemented in the on-board FPGA.

4.8 FPGA for PCI Arbiter & Versaclock Controller

A small auxilliary FPGA on the board is included to provide PCI arbiter functionality and to program the on-board clock conditioning circuits for Ethernet and SDRAM via an I2C sequencer.

This FPGA is an Actel Igloo Nano *AGLN125V2* in a 100 VQFP package. The JTAG chain for this device is separate from the *GR740* JTAG, and for programming the device a separate Actel style 10 pin connector suitable for a FlashPRO4 programming cable is foreseen (*J13).*

The FPGA is pre-programmed on delivery and is designed to function on power up without any user interaction.

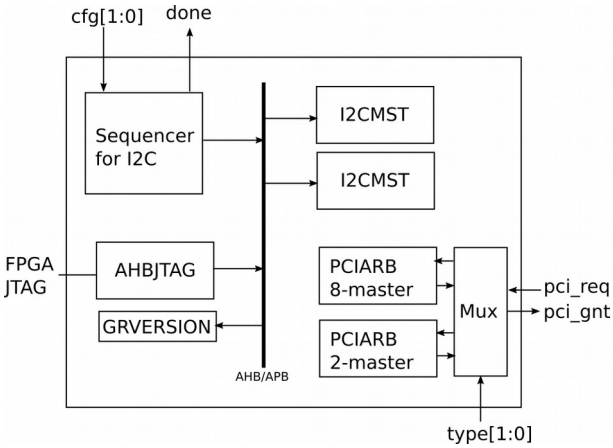


Figure 4-20: Block Diagram of the Auxiliary FPGA functions

For the PCI arbiter function, a mode input signal is used to configure the routing of signals to work in the four different configurations (direct/bridge, host/peripheral). This gets automatically set by the plug-in boards for PCI to match the set configuration.

The clock circuits are programmed automatically on reset by a sequencer built into the FPGA that sends commands over I2C to the clock circuits. For the programming, the configuration jumpers JP24 need to be set to match the intended SDRAM clock frequency according to below table:

SDCLK-Freq Range	JP24, 3-4	JP24, 1-2
50-60 MHz	'0' => install	'0' => install
60-71 MHz	'0' => install	'1' => open
70-83 MHz	'1' => open	'0' => install
83-100 MHz	'1' => open	'1' => open

Table 3: SD-CLK Frequency Range Jumper Settings

Since the default board configuration generates 100 MHz SDRAM clock (50 MHz oscillator multiplied by 2 by ASIC PLL), the board is delivered with both JP24 jumpers disconnected.

4.9 Spacewire (LVDS) Interfaces

The GR740 processor provides nine Spacewire interfaces which are routed to the front panel of the board.

Eight of the Spacewire interfaces form an 8-port SpaceWire router/switch with four on-chip AMBA ports with RMAP. The board supports a link rate for SpaceWire up to 200 Mbit/s.

The ninth SPW port is dedicated as a SPW Debug interface, as part of the DSU functionality. The maximum link rate for this port is 100 Mbit/s

4.9.1 SPW interface circuit

Each Spacewire interface consists of 4 LVDS differential pairs (2 input pairs and 2 output pairs).

With the exception of the SPW-DBG interface, the Spacewire interfaces to the *GR740* ASIC are LVDS and do not require additional LVDS transceiver devices. The SPW_DBG signals are shared with GPIO functions, and are LVCMOS (3.3V logic) and required an LVDS driver and receiver circuit.

The PCB traces for the LVDS signals on the GR-CPCI-GR740 board are laid out with 100-Ohm differential impedance design rules and matched trace lengths.

100 Ohm Termination resistors for the LVDS receiver signals are mounted on the board close to the receiver.

4.9.2 SPW Connectors

In order to be compatible with other SPW equipment, standard MDM9S connectors are mounted on the CPCI front panel for the Spacewire interfaces. The pin out of the MDM9S connectors for these Spacewire interfaces conform to the Spacewire standard. In order to make the transition from the PCB to the front panel, 40 pin high speed SAMTEC connectors together with a small flex-prints are used, as shown in Figure 4-21.

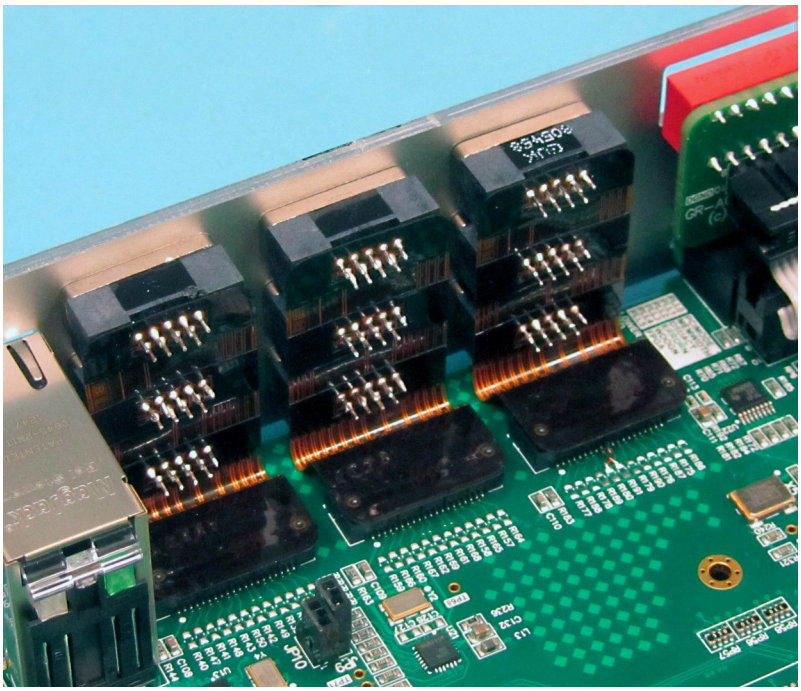


Figure 4-21: SPW flex connection

4.9.3 SPW connector implementation details and precautions to follow

This equipment has SPW ports that use Low Voltage Differential Signalling (LVDS) which has limited common mode voltage protection.

Before plugging the SPW cable between two equipments please power up and make sure that there is no voltage difference between their grounds.

The SPW standard specification specifies that the cable side outer-shield is bonded to the connector shell, but does not say anything about the grounding/bonding of the connector side shell. In this equipment the SPW connector side shell are by default bonded to the front panel/box local chassis but not bonded to the local GND of the SPW circuits.

The pin 3 of this equipment's SPW connectors are connected to the GND through a parallel capacitor (100p) and resistor (10k) network. When connected to a SPW cable (properly designed as per the standard) the pin 3 will be connected to its inner shield. Note the inner shield does not provide end to end ground connection between two equipments as per the SPW standard.

In this equipment there is no grounding provided via the SPW connectors (neither through pin 3 inner shield nor through connector side shell between two equipments). The users connecting the board to other equipment only via SPW should ensure grounding via other means (e.g. a dedicated wire).

4.10 FTDI Serial to USB Interface

To provide additional flexibility, an FTDI FT4232HL Serial to USB interface chip is provided on board.

This device provides four Ports which connect to a single Mini-AB USB connector (J1) on the front panel. This USB port can be connected to a host computer to allow communication over serial interfaces to Host PC's which do not have conventional 9 pin D-sub type RS232 connectors.

Additionally, the FTDI FT4232HL chip is also able to perform a JTAG to USB conversion function.

As represented in Figure 4-22, sets of jumpers allow a number of possibilities to be configured:

1. Connect JTAG to FTDI Port-A
2. Use JTAG on 6-pin 0.1” Header
3. Connect Power Measurement I2C interface to FTDI Port-B
4. Connect to Power Measurement I2C on 6-pin 0.1” Header
5. Connect UART0 to FTDI port C
6. Connect UART0 via the header with an external RS232 circuit
7. Connect UART1 to RS232 connector J7
8. Connect UART1 via the header with an external RS232 circuit

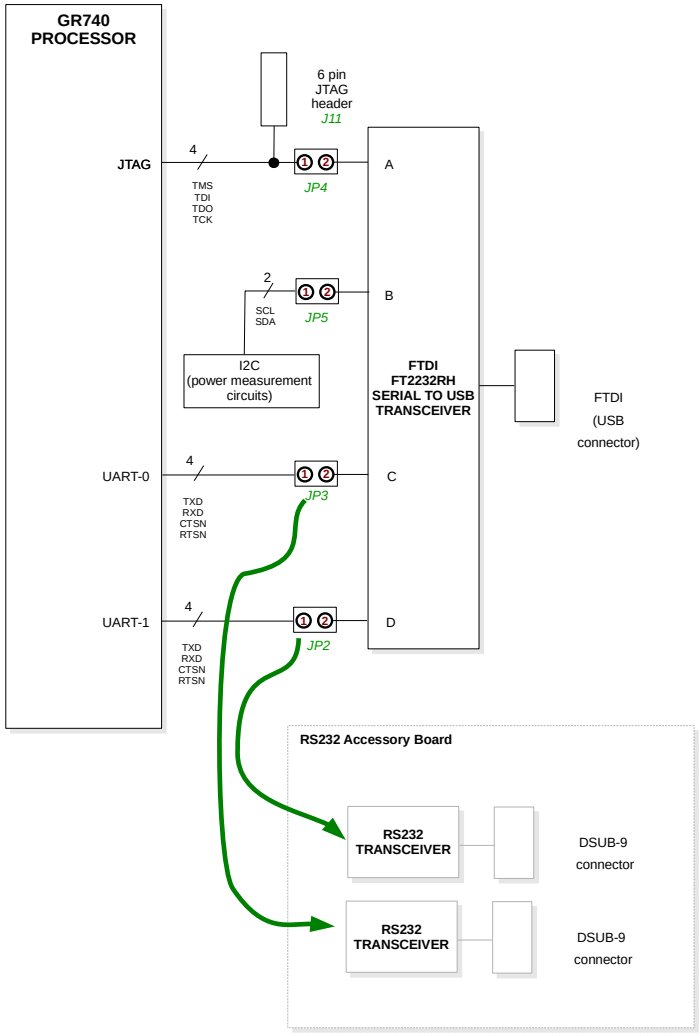


Figure 4-22: Block diagram of FTDI Serial/JTAG to USB Interface

Please note that the UART interface shares pins with PROM/IO interface. See [RD1] section 3.3 Pin multiplexing for information on how to correctly configure the pin multiplexing between UART and PROM/IO signals.

4.11 SPI interface

The GR740 processor also provides an SPI interface for user defined devices.

As shown in Figure 4-23 , the SPI interface pins of the GR740 processor are connected to a 10 pin 0.1” header on the board to allow an external circuit SPI circuits to be hooked-up.

As an example SPI circuit, the GR-CPCI-GR740 Board provides an AD7814, Temperature monitor circuit on the board, which is selected with the *SPI_SLVSEL0* output of the ASIC. If the *SPI_SLVSEL0* signal is to be used for an external SPI circuit,

then the jumper *JP8* must be removed to disable the on-board SPI circuit.

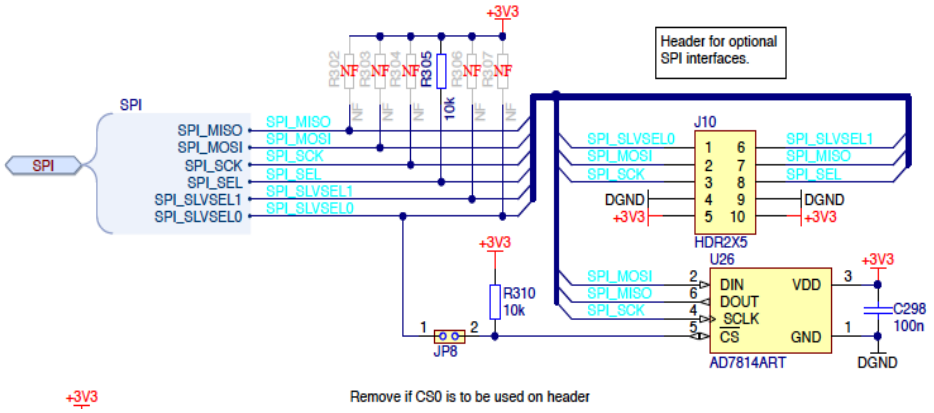


Figure 4-23: SPI Interface Configuration

4.12 GPIO

The GR740 processor provides 16 general Purpose Input Output signals (3.3V LVCMOS voltage levels).

The 16 general Purpose Input Output signals of the ASIC (3.3V LVCMOS voltage levels) are connected to a set of 0.1” pitch pin header connector on the front panel thus

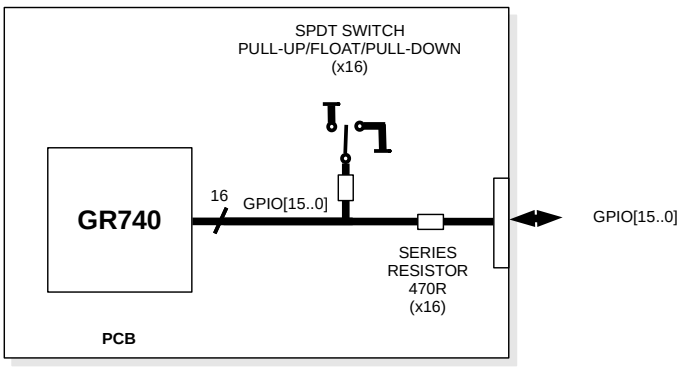


Figure 4-24: GPIO interface

allowing easy access to these signals, either individually, or with a ribbon cable connection. A series protection resistor of 470 Ohm is included on each signal at the front panel connector.

A single-pole-double-throw DIP switch allows a weak (47k) pull-up or pull-down to be configured on each of the GPIO signals lines on the PCB and allows the user to conveniently set the signal state when the GPIO lines are configured as inputs. When programmed as outputs the DIP switches should be left in the 'open' ('float') state.

Note that the state of the GPIO pins is sampled at power-up or reset of the processor in order to determine initial conditions of a number of internal features, as listed in the

Table 4.

To ensure the correct initialisation of the processor, the user should ensure that the initial DIP switch settings are correctly set to set the users' required configuration at power up or reset of the board. After reset, the GPIOs can be used as normal I/Os.

In particular, since this board has a configurable 16 bit or 8 bit prom interface, the setting of GPIO[10] should be consistent with the setting of Jumper JP6 pins 11-12 (installed = 8 bit; uninstalled = 16 bit interface) in order that the board can successfully execute its program from Prom at start up.

GPIO	Function	Comment
0	EDCL LINK0 & 1 MACADDR Bit 0	DIP Switch Closed = '0'; Open = '1'
1	EDCL LINK0 & 1 MACADDR Bit 1	DIP Switch Closed = '0'; Open = '1'
2	EDCL LINK0 MACADDR Bit 2	DIP Switch Closed = '0'; Open = '1'
3	EDCL LINK0 MACADDR Bit 3	DIP Switch Closed = '0'; Open = '1'
4	EDCL LINK1 MACADDR Bit 2	DIP Switch Closed = '0'; Open = '1'
5	EDCL LINK1 MACADDR Bit 3	DIP Switch Closed = '0'; Open = '1'
6	SPW Router Int. Mode Bit 0	Together with bit 7 Selects SpaceWire router Distributed Interrupt configuration, acc Table 23 of [RD1]: "00" - Interrupts with acknowledgement mode (32 interrupts with acknowledgements); "01" - Extended interrupt mode (64 interrupts, no acknowledgements); "10" - Distributed interrupts disabled, all Dist. Interrupt codes treated as Time-Codes; "11" - Dist. interrupt disabled, Control code treated as Time-Code if CTRL flags are zero.
7	SPW Router Int. Mode Bit 1	See above.
8	EDCL LINK0 TRAFFIC	DIP Switch Closed = '0'=>MASTER AHB; Open = '1' => DEBUG AHB
9	EDCL LINK1 TRAFFIC	DIP Switch Closed = '0'=>MASTER AHB; Open = '1' => DEBUG AHB
10	PROM WIDTH	DIP Switch Closed = '0' => 8 bit ; Open = '1' => 16 bit Note: the setting of GPIO[10] should be consistent with the setting of Jumper JP6 pins 11-12 (installed = 8 bit; uninstalled = 16 bit interface)
11	SPW Router clock-gating	DIP Switch Closed = '0' => Core enabled; Open = '1' => Core disabled.
12	SPW ROUTER ID BIT 0	DIP Switch Closed = '0'; Open = '1'
13	SPW ROUTER ID BIT 1	DIP Switch Closed = '0'; Open = '1'
14	PROM EDAC	DIP Switch Closed = '0' => Disable; Open = '1' => Enable
15	PROM/IO I/F	DIP Switch Closed = '0' => Enable; Open = '1' => Disable Selects if the PROM/IO interface should be enabled after reset. If this signal is '0' then the PROM/IO interface is enabled. Otherwise the PROM/IO interface pins are routed to their alternative functions. See §3.2.1 of [RD4]**.** This bit does not affect board functionality, the board jumpers also need to be configured appropriately to enable the PROM (Flash)

Table 4: GPIO Definitions

4.13 Bootstrap Signals

Additionally, a front-panel DIP switch, FP-S3, is provided to allow the user to conveniently set the state of the functions listed in the table below:

Switch	Function	Comment
1	DSU Enable	DIP Switch Closed = '0' => DISABLE; Open = '1' => ENABLE
2	MEM_CLKSEL	Select source of memory clock: Closed = '0' => Same source as SYSCLK Open = '1' => MEM_EXTCLOCK
3	BYPASS_PLL0	Bypass PLL of SPW Clock: Closed = '0' => PLL operates Open = '1' => PLL Bypassed
4	BYPASS_PLL1	Bypass PLL of SDRAM Clock: Closed = '0' => PLL operates Open = '1' => PLL Bypassed
5	BYPASS_PLL2	Bypass PLL of System Clock: Closed = '0' => PLL operates Open = '1' => PLL Bypassed
6	PLL_IGNLOCK	Ignore PLL lock status when generating reset in GR740 Closed = '0' => PLL lock status affects reset operation Open = '1' => Ignore PLL lock status
7	ETH_CLK	Set Ethernet interface mode Closed = '0' => 100 Mbit mode Open = '1' => Gbit interface mode
8	WATCHDOG	DIP Switch Closed => Watchdog can reset processor. DIP Switch Open => Watchdog can not reset processor.

Table 5: DIP Switch S3 Definitions

4.14 Accessory Board Circuits

Due to limited front panel space, some of the 'optional' interfaces are accommodated by a separate accessory board with a separate one-slot front panel.

The following features are installed on this accessory board which is connected to the GR-CPCI-GR740 board with an appropriate ribbon cable:

- Dual CAN 2.0 Interfaces
- Dual MIL-1553 Interfaces
- Dual RS232 (UART) interfaces

Note that the interface pins that drive these features are dual purpose pins shared with the PROM interface (ref. Section 4.5.3). In order to use these interfaces, it is therefore necessary to a) understand the possible restrictions and conflict with the PROM operation, and b) to ensure that the internal function registers of the *GR740* are correctly set up.

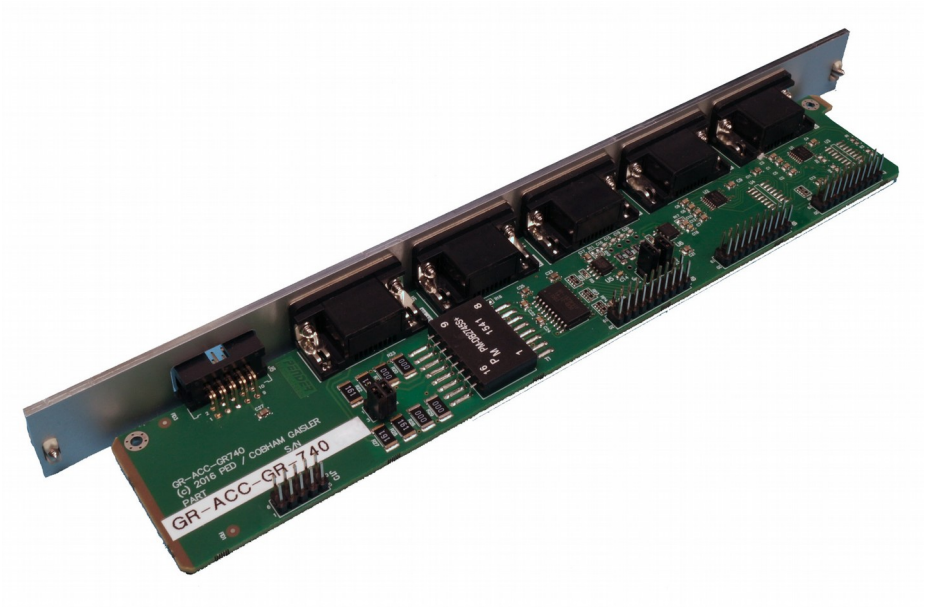


Figure 4-25: GR-ACC-GR740 Accessory Board

4.14.1 CAN 2.0 Interfaces

The PCB provides the electrical interfaces for two CAN bus interfaces, as represented in the block diagram, Figure 4-26.

The CAN bus transceiver IC's on this board are *SN65HVD230* devices from Texas Instruments which operate from a single +3.3V power supply.

D-sub 9 pin connectors are provided on the front panel.

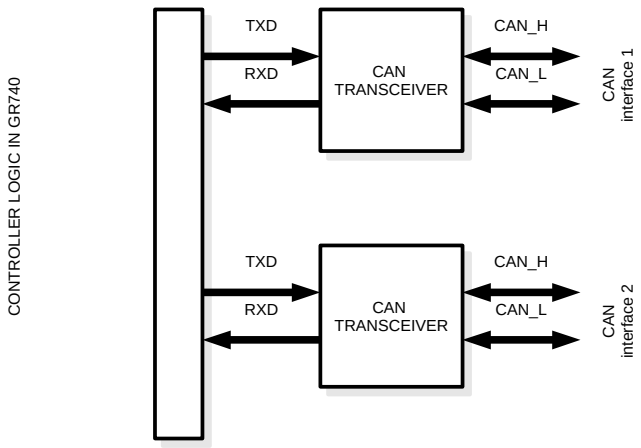


Figure 4-26: Block Diagram of the CAN interface

4.14.1.1 Configuration of Bus Termination

The CAN interfaces on the board can be configured for either end node or stub-node operation by means of the *Accessory Board* jumpers JP1 and JP2 for interface 1 and 2 respectively, as shown in Figure 4-27.

For normal end-node termination with a nominal 120 Ohm insert jumpers in position 1-3.

However, if a split termination is desired (if required for improved EMC performance), insert the jumpers in positions 1-2 and 3-4.

For stub nodes, if termination is not required, do not install any jumpers.

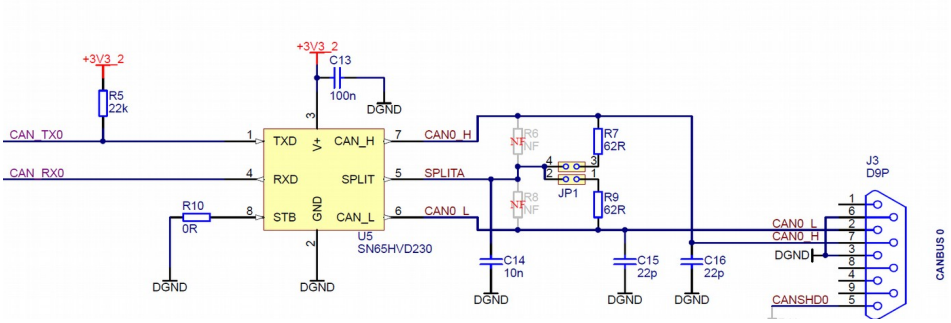


Figure 4-27: Transceiver and Termination Configuration (one of 2 interfaces shown)

A further feature provided by the SN65HVD230 device is the capability to adjust the transceiver slew rate. This can be done by modifying the values of resistors connected to pin 8 of the transceivers.

The default value of 0 Ohms is compatible with 1Mbps operation.

From the data sheet the following resistor values give the following slew rates:

10kOhm => 15V/us

100kOhm => 2V/us

4.14.2 MIL-STD-1553 Interface

The board implements a Dual MIL-STD-1553 interface with a 3.3V Transceiver and Transformer circuits as shown in Figure 4-28.

The default configuration of the board supports Long-Stub Coupling configuration. However, short-stub and direct-coupling can also be supported depending on the configuration of resistors which is soldered to the board (see Figure 4-28). Additionally, an 80 Ohm parallel termination can be installed if the 2 pin jumpers are installed.

Since there are various 'standard' connectors defined for the connection to MIL-STD-1553 bus, and because of limited PCB and front panel area, it a D-sub 9-Male connector on the front panel to accommodate both the A and B bus connections. A D-sub 9-Male

connector on the front panel is selected as this can be most easily adapted to suit the user's desired connector configuration.

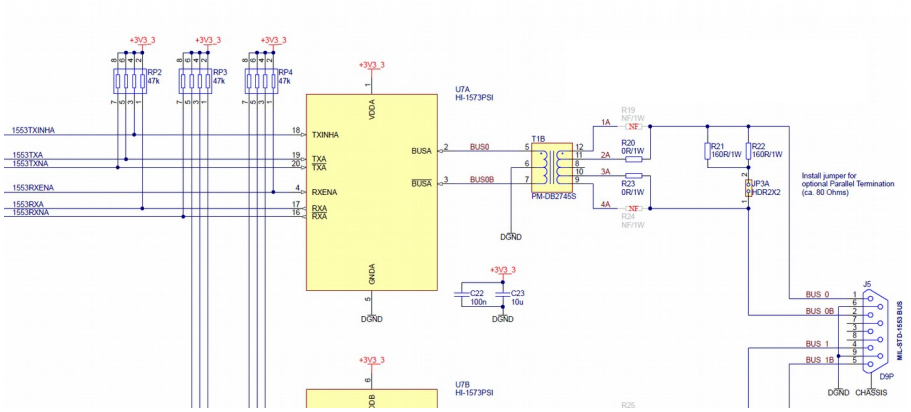


Figure 4-28: MIL-STD-1553 Transceiver and Transformer circuit

(one of two interfaces shown)

Note: Concerning routing on the PCB: Underneath the transformer and associated traces of the MIL-1553 circuit, the PCB planes in the internal layers have been 'removed', and no other traces are routed through this area of the PCB. This is done in order to eliminate any magnetic coupling from the transformer circuit in to the Ground plane.

4.14.3 Serial Interface (RS232)

The accessory PCB provides RS232 interface circuits for two Serial interfaces with TXD/RXD/CTSN/RTSN pins.

The RS232 transceiver IC's on this board are SN75C3232 devices from Texas Instruments which operate from a single +3.3V power supply.

The front panel incorporates standard Female D-Sub 9 pin type connector with a standard pin-out for serial links.

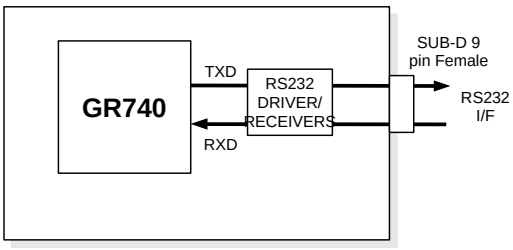


Figure 4-29: Serial interface

Note: As explained in section 4.10, the serial interfaces of the GR740 processor can either be connected to these front panel connectors (RS232) or to the FTDI-USB interface chip, depending on the setting of the jumpers JP17 to JP28. The user should

take care to set the appropriate jumper configuration depending on the configuration required.

4.15 Debug Support Unit Interfaces

Program download and debugging to the processor is performed using the GRMON3 Debug Monitor tool from Frontgrade Gaisler (RD-5). The GR740 processor provides an interface for Debug and control of the processor by means of a host terminal via its DSU interface, as represented in Figure 4-30.

Three control signals and a data connection from the Debug Support Unit interface to the processor:

DSUEN: This signal is pulled high on the board to enable Debugging

The signal can be pulled low with DIP Switch S3-1 to disable the DSU. Switching off the DSU also sets the clock gating to off for all the debug interfaces (SpaceWire, JTAG and Ethernet interfaces connected to debug subsystem).

DSUBRE: The push-button switch S4 pulls the DSUBRE signal high to force the processor to halt and enter DSU mode.

DSUACT: When the processor is halted, the LED will illuminate

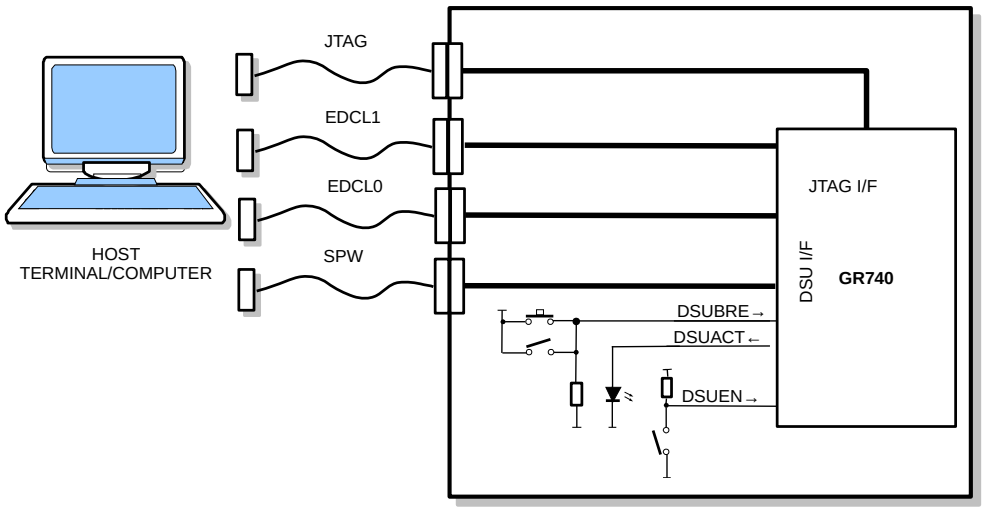


Figure 4-30: Debug Support Unit connections

To communicate with the processor, three possibilities for the data connection to the processor are provided:

SPW-DSU	Spacewire Debug Communication Link (connector J2a)
JTAG-DCL	JTAG Debug Communication Link (connector J11 or J1 through FTDI interface)
EDCL	Ethernet Debug Communication Link (connector J1A (Upper) or J1B

(Lower))

GRMON3 can be used with the above listed interfaces. For more information, please refer to [RD4].

4.16 Other Auxiliary Interfaces and Circuits

4.16.1 Oscillators and Clock Inputs

The oscillator and clock scheme for the *GR-CPCI-GR740* Board is shown in Figure 4-31.

The main oscillator providing the *SYS_CLK* for the *GR740* ASIC.

To enable different oscillator frequencies to be used, a DIL socket is provided which accepts 4 pin DIL8 style 3.3V oscillator components.

Additionally, oscillators are provided as follows:

- DIL Socket with 33/66 MHz oscillator and zero delay buffer circuit for PCI interface and slots
- DIL Socket for 50 MHz oscillator to provide a separate clock for the SDRAM Memory interface
- DIL Socket for 50 MHz oscillator to provide a separate clock for the Spacewire interfaces
- 20 MHz oscillator (Fixed SMD soldered on board) for the MIL-STD-1553 clock
- 12MHz crystal which generates local oscillator for FTDI-USB interface
- 25 MHz crystal with a Versaclock programmable clock generator for generating the GTX Clocks with adjustable phase required for the two GMII Ethernet interfaces

Internally to the ASIC, PLL circuits generate the required clock frequencies and phases for the following:

- Processor Main frequency
- SDRAM Clock
- Spacewire Clock

For more details of the internal PLL structure and clock gating and multiplexing features of the *GR740*, please refer to [RD4].

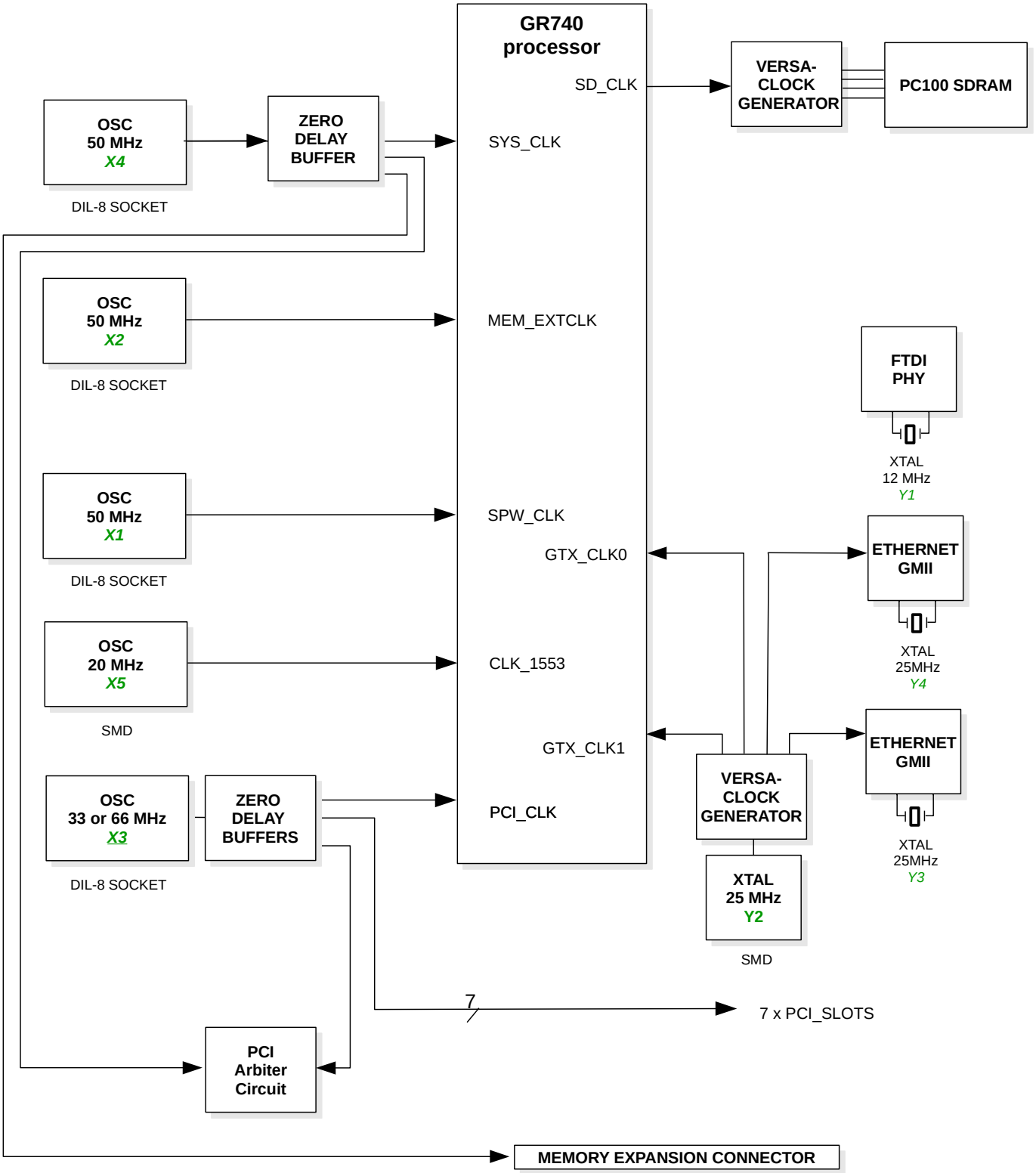


Figure 4-31: Board level Clock Distribution Scheme

4.16.2 Power Supply and Voltage Regulation

A single power supply with a +5V (nominal) / +12V (maximum) is required to power the board. All other necessary voltages on the board are derived from this input using discrete Power circuits on the board (DC/DC or Linear Regulators as appropriate).

On board regulators generate the following voltages:

- +3.3V for the GR-CPCI-GR740 I/O voltage, interfaces and other peripherals
- +2.5V for GR740 SPW interface I/O voltage
- +1.2V for GR740 Vcore voltage & PLL Digital power supplying
- Linear regulated +1.2V supply for GR740 PLL Analog power supplying

Appropriate decoupling capacitance is provided for all the supply voltages.

The Power Supply structure is significantly over-dimensioned using 10A power modules (PTH08T240W) as the basis, in order to provide for uncertainty and flexibility. The advantage of the selected DCDC power modules is their ease of implementation and the wide allowable input voltage range (+4.5V to +14V).

Input Voltage

The nominal input voltage for the board is +5V. This input voltage can be connected either to the 2.1mm Jack connector, J14 on the board, or taken from the +5V PCI rail from the PCI Backplane. An additional power input connector J15 is provided on the board, as an alternative to the connector J14. This could be useful as a more convenient connection in the situation that the board would be built in to a 'stand-alone' equipment housing.

Note: You must not apply power to the connector J14/J15 when the board is plugged into a CPCI rack.

Note: Since the DCDC power modules used have a wide allowable input voltage range (+4.5V to +14.5V), it is acceptable to supply the board via the J14 connector from any voltage supply in the range +5V to +12V. However, the term '+5V nominal' is used in this description since this is the voltage which the Compact PCI backplane will supply when the board is plugged into a CPCI rack.

Power Sequencing

Automatic power-sequencing is implemented on the board. In order to reduce in-rush current, which may damage the GR740 it is required to power up in the following sequence:

1. Raise I/O voltage rails (3.3V single-ended and 2.5V for LVDS) in any order
2. Raise 1.2V core supply and PLL 1.2V digital supplies
3. Raise PLL 1.2V analog PLL supply
4. Raise sys_resetn once clocks are stable

In order to achieve this power sequencing, the GR740 processor board implements a small power sequencer circuit (ISL8702). This circuit provides four open drain output flags which are connected to the TRACK pins of the DCDC modules. On power up, the output flags are sequentially released in a timed sequence (ca. 10 ms spacing, using a 10nF capacitor on the *TIME* pin).

The first flag controls the start-up of the VIO (+3.3V and 1.8V) DCDC converters.

The second flag controls the start-up of the Vcore (+1.2V) DCDC converter.

The third flag controls the enable pin of the 1.2V linear regulator for the Analog PLL voltage

The fourth flag is unused in this configuration

The output flags will follow a reverse sequence during power down to avoid latch conditions.

CPCI +/-12V Supply

The +12V and -12V (500mA max) power supply which the compact PCI can provide via the Backplane is not used on this board. However, these +12V/-12V connections are connected to the Memory Expansion connector, J9, in case this could be useful for supplying circuits on User Defined mezzanine boards mated to J9. Note though, that in the case that the board is not powered via the CPCI backplane, that these pins will be unpowered.

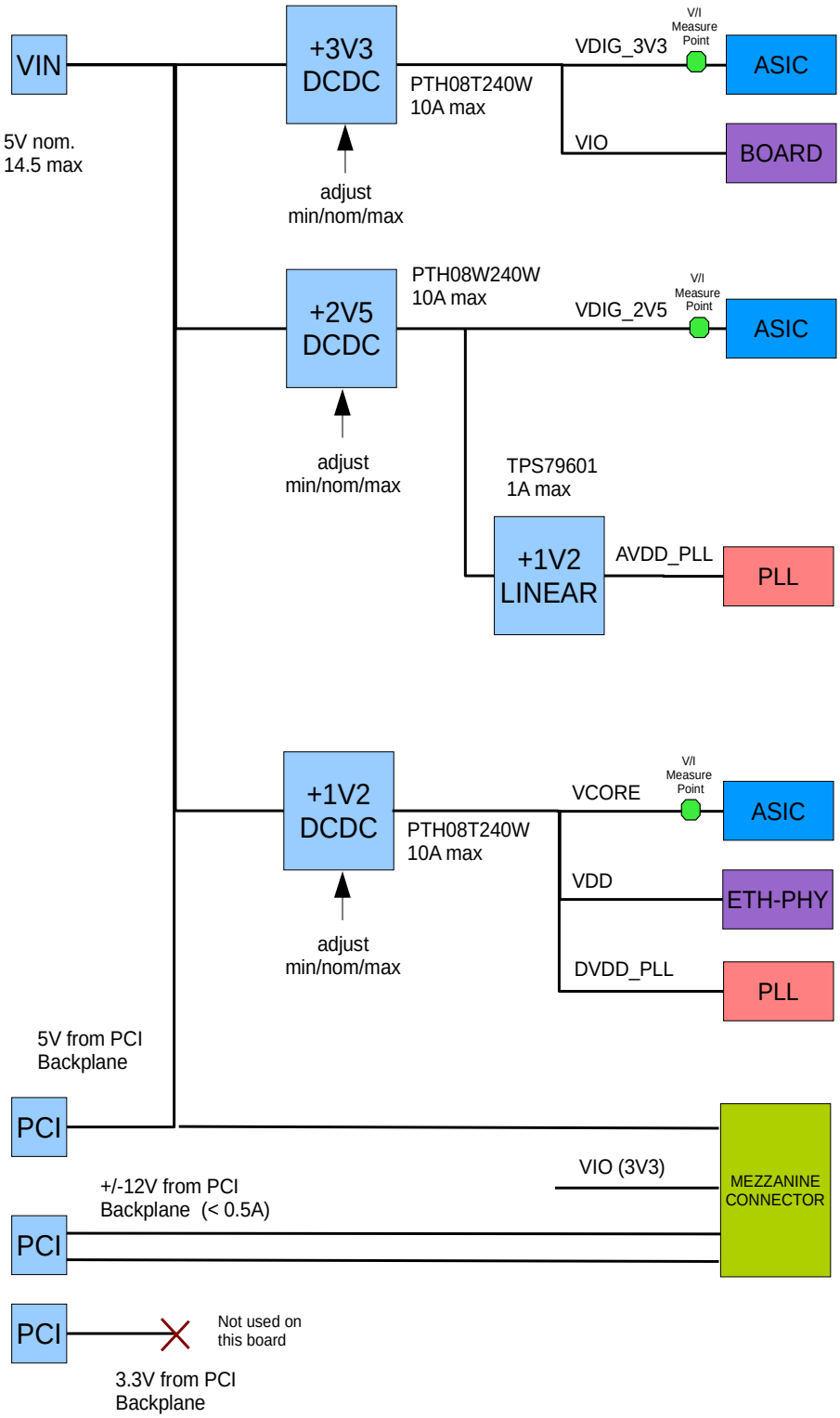


Figure 4-32: Power Regulation Scheme

4.16.3 Reset Circuit and Button

A standard Processor Power Supervisory circuit (TPS3705 or equivalent) is provided on the Board to provide monitoring of the 3.3V power supply rail and to generate a clean reset signal at power up of the Unit.

To provide a manual reset of the board, a miniature push button switch is provided on the Main PCB for the control. Additionally, connections are provided to an additional off-board push-button RESET switch if this is required.

This reset device has a fixed delay time of nominal duration 200ms (range specified in datasheet: 140ms to 280ms)

4.16.4 Watchdog

The GR740 processor includes a Watchdog timer function which can be used for the purpose of generating a system reset in the event of a software malfunction or crash.

On this development board the WDOGN signal is connected as shown in the Figure 4-33 to the Processor Supervisory circuit.

To utilise the Watchdog feature, it is necessary to appropriately set-up and enable the Watchdog timer. Please consult the GR740 processor User Manual ([RD1]) for the correct register locations and details.

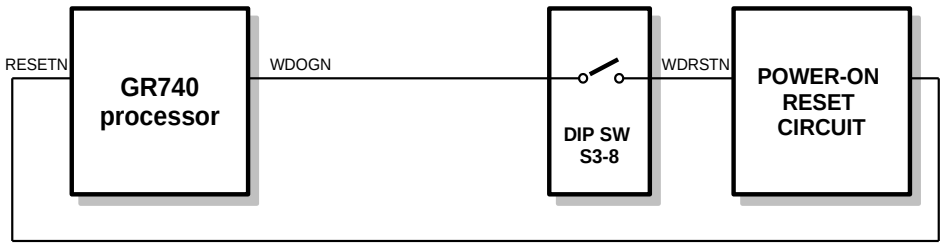


Figure 4-33: Watchdog configuration

Also, to allow the WDOGN signal to generate a system reset it is necessary to 'close' the DIP Switch FP-S3-8 (see Table 5).

For software development it is often convenient or necessary to disable the Watchdog triggering in order to be able to easily debug without interference from the Watchdog operation. In this case, the DIP Switch S3-8 should be 'open'. When the watchdog triggers, a system reset will not occur. However, the Watchdog LED, D19 will still illuminate.

4.16.5 JTAG interface

Connector J11, a 6 pin 0.1” header connector provides the JTAG connection for a Digilent Style JTAG cable, or with flying leads to a Xilinx Style JTAG cable.

This interface allows DSU Debug over the JTAG interface to be performed.

4.17 Heatsink/Fan

Sufficient space is provided around the periphery of the *GR740* to allow either a passive or fan-heatsink to be mounted, for passive or active cooling of the *GR740*, if required.

A suitable passive passive heatsink for the 29x29 mm BGA housing with approximately 15mm height could be:

INM29001-15W/2.6, from Radian Heatsinks

Alternatively, a suitable fan heatsink could be similar to:

ATS-61290D-C1-R0 (requires separate fan) from Advanced Thermal Solutions

These types of heatsink can be most suitably attached to the ASIC with an adhesive pad, and do not require any additional tooling holes to be drilled in the PCB.

In order to be able to power an active Fan-Heatsink, a 0.1” pitch two pin header, JP13, is provided on the board. This header provides +VIN and DGND connections. The selected Fan should be compatible with the input voltage which is being provided to the board (range 5V to 14V). There is no active monitoring and control of the heatsink-fan provided.

5 Setting Up and Using the Board

The default status of the Jumpers and Switches on the boards is as shown in Table 6 and Table 7. (Other configurations may be defined by the user).

For additional information, refer to Table 6 and for information about the Bootstrap signals, refer to Table 23 of [RD1].

Jumper	Jumper Setting	Comment
JP1	Connected to Front-Panel	Connects front panel RESET and BREAK switch to JP1
JP2	Not installed (4x)	UART1 not connected to FTDI chip
JP3	Not installed (4x)	UART0 not connected to FTDI chip
JP4	1-2 3-4 5-6 7-8	Connects ASIC JTAG to FTDI chip
JP5	1-2 3-4	Connects I2C to FTDI chip
JP6	3-4 5-6 7-8 9-10 11-12 (1-2 open)	Configured for 8 bit Flash memory PROM
JP7	Not installed (4x)	GPIO[7..4]; For SPW-DSU install 1-2 and 3-4
JP8	1-2	SPI-OB; Install to enable on-board SPI circuit
JP9	Installed 1-2	VC0-CLKSEL; XTAL generates 25MHZ clock
JP10	Not installed	VC0-PROG, do not install for parameters to be loaded via I2C
JP11	Jumpers 1,2,13 &14 in position C-D Other jumpers in position A-B (18x)	Install A-B for PROM and C-D for alternate I/F functions. See Table 1 for individual pin description. Other configurations are possible, but require care: see section 4.5.3.
JP12	Do not install	+3.3V
JP13	Do not install	+VIN
JP14	Install	I3V3asic
JP15	Install	I2V5
JP16	Install	I1V2
JP17	Open	TESTEN disabled
JP18	Open	PCI bus runs at 33MHz
JP19	Not installed	PCI_RSTN configuration options
JP20	Not installed	VC1-CLKSEL; SD_CLK generates SDCLK's
JP21	Not installed	VC1-PROG, do not install for parameters to be loaded via I2C
JP22	Install	BP-CLK (Host Mode) all clocks present on BP
JP23	Install	M66EN; Force backplane to 33MHz
JP24	Not installed	Configuration options for Versaclock PLL ranges

Table 6: Default Setting of Jumpers

Switch	GPIO	Switch Setting	Comment
FP-S1-1 to 6	GPIO[5..0]	Open = '1'	GPIO[5..0] Mac address. Default = Disable EDCL
FP-S1-7 & 8	GPIO[7..6]	Open = '1'	SPW Router INT mode. Default = Pulled up.
FP-S2-1 & 2	GPIO[9..8]	Open	EDCL0 & EDCL 1 Link traffic : EDCL Enabled
FP-S2-3	GPIO[10]	Closed	PROM Width = 8 bit
FP-S2-4	GPIO[11]	Open	'1' => Disables SPW Router
FP-S2-5 & 6	GPIO[13..12]	Open	SPW Router ID = '11'
FP-S2-7	GPIO[14]	Closed	PROM EDAC disabled
FP-S2-8	GPIO[15]	Closed	PROM I/O enabled
FP-S3-1		Open	DSU Enabled
FP-S3-2		Open	MEM-CLK is taken from Xtal X2
FP-S3-3		Closed	PLL for SYS_CLK enabled (‘Open’ for 'bypass')
FP-S3-4		Closed	PLL for MEM_CLK enabled (‘Open’ for 'bypass')
FP-S3-5		Closed	PLL for SPW_CLK enabled (‘Open’ for 'bypass')
FP-S3-6		Open	Disable PLL lock
FP-S3-7		Closed	Ethernet Clock: 100M Ethernet on ETH-0 and ETH-1
FP-S3-8		Open	WD output does not cause board reset

Table 7: Default Setting of Switches

To operate the unit stand alone on the bench top, connect the +5V power supply to the Power Socket J14 at the back of the unit. (centre-pin is +ve).

ATTENTION! To prevent damage to board, please ensure that the correct power supply voltage and polarity is used with the board.

Do not exceed +14.5V at the power supply input, as this may damage the board.

The POWER LED should be illuminated indicating that the +3.3V power is active.

Upon power on, the Processor will start executing instructions beginning at the memory location 0xc0000000, which is the start of the PROM. If the PROM is 'empty' or no valid program is installed, the first executed instruction will be invalid, and the processor will halt with an ERROR condition, with the ERROR LED illuminated.

To perform program download and software debugging on the hardware it is necessary to use the Frontgrade Gaisler GRMON3 debugging software, installed on a host PC (as represented in Figure 4-30). Please refer to the GRMON3 documentation for the installation of the software on the host PC (Linux or Windows), and for the installation of the associated hardware dongle.

To perform software download and debugging on the processor, a link from the Host computer to the DSU interface of the board is necessary. As described in section 4.15 there are four possible DSU interfaces available on this board:

SPW-DSU	Spacewire Debug Communication Link (connector J2a if JP11 and JP7 set)
JTAG-DCL	JTAG Debug Communication Link (connector J11 or J1 through FTDI interface)
EDCL	Ethernet Debug Communication Link (connector J1A (Upper) or J1B (Lower))

Program download and debugging can be performed in the usual manner with GRMON3. More information on the usage, commands and debugging features of GRMON3, is given in the GRMON3 Users Manuals and associated documentation.

6 Interfaces and Configuration

Note: In the case of any discrepancy, please refer to the schematic ([RD2]) as the 'golden' source for the connector and pin out information.

6.1 List of Connectors

Name	Function	Type	Description
J1	FTDI-USB	USB-MINI-AB	Configurable serial to USB I/F via FTDI chip acc. §4.10
J2a-i	9-port SPW	MDM9S	9 x SPW interfaces (incl .SPW-DSU)
J3A	ETH-1	Dual RJ45-Top	10/100Mbit/s Ethernet Connector 1
J3B	ETH-0	Dual RJ45-Bottom	10/100Mbit/s Ethernet Connector 0
J4	GPIO[15..0]	2x17pin 0.1” Header	Header for ribbon cable to 16 x GPIO
J5	DIP-SW	10 pin 0.1” Header	Header for ribbon cable to Front panel DIP Switch
J6	DUAL	2x10pin 0.1” Header	Header for ribbon cable to 2 x UART I/F
J7	CAN	2x10pin 0.1” Header	Header for ribbon cable to 2 x CAN I/F
J8	MIL-1553	2x10pin 0.1” Header	Header for ribbon cable to 2 x MIL1553-I/F
J9	MEM_EXT	AMP 5177984-5	Memory Interface signals
J10	SPI	2x5pin 0.1” Header	Header for SPI signals
J11	JTAG-ASIC	6 pin 0.1” Header	JTAG interface for GR740
J12	JTAG-PCI	6 pin 0.1” Header	JTAG interface for PCI Bridge circuit
J13	JTAG-FPGA	2x5pin 0.1” Header	JTAG interface for Microsemi/Actel FPGA
J14	POWER-IN	2.1mm center +ve	+5V DC power input connector
J15	POWER-IN'	Mate-N-Lok 4pin	Alternative power input for 4 pin IDE style connector
J16	SDRAM	SODIMM144	SDRAM[79..64] & [31..0] (Top Side connector)
J17	SDRAM	SODIMM144REV	SDRAM[95..80] & [63..32] (Bottom Side connector)
J18	SYS-CLK	MMCX-jack	Coaxial connector for injecting alternative SPW-CLK
J19	MEM-CLK	MMCX-jack	Coaxial connector for injecting alternative MEM-CLK
J20	SPW-CLK	MMCX-jack	Coaxial connector for injecting alternative SYS-CLK
J21	CONFIG1	HIROSE-FX11LA-120S/12	Configuration plug for 96bit SDRAM configuration
J22	CONFIG2	HIROSE-FX11LA-120S/12	Configuration plug for 48bit SDRAM + ETH1 I/F

Name	Function	Type	Description
J23	CONFIG3	HIROSE-FX11LA-120S/12	Configuration plug for 48bit SDRAM + PCI I/F
J24	BRIDGE-X	HIROSE-FX11LA-60S/6	PCI Bridge Mezz.– connections to GR740
J25	BRIDGE-P	HIROSE-FX11LA-60S/6	PCI Bridge Mezz.– connections to Bridge-Primary
J26	BRIDGE-S	HIROSE-FX11LA-60S/6	PCI Bridge Mezz.– connections to Bridge-Secondary
J27	BRIDGE-Y	HIROSE-FX11LA-60S/6	PCI Bridge Mezz.– connections to PCI c backplane
J28	ARBITER	HDR2X10_2mm	Test Header for Arbiter GNT/REQ signals
J29	SD_CLK	MMCX-jack	Clock Monitor/Test-point
J30	SD_CLK0	MMCX-jack	Clock Monitor/Test-point
J31	SD_CLK1	MMCX-jack	Clock Monitor/Test-point
J32	SD_CLK2	MMCX-jack	Clock Monitor/Test-point
J33	SD_CLK3	MMCX-jack	Clock Monitor/Test-point
J34	SD_CLK_FB	MMCX-jack	Clock Monitor/Test-point
CPCI-J1	CPCI	CPCI Type A	CPCI connector
CPCI-J2	CPCI	CPCI Type B	CPCI connector

Table 8: List of Connectors

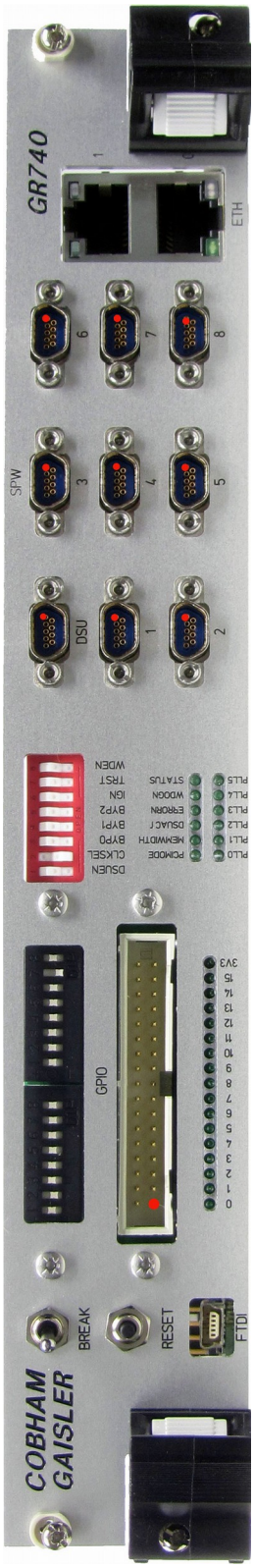


Figure 6-1: Front Panel View (pins 1 marked red)

Pin	Name	Comment
1	VBUS	+5V (from external host)
2	DM	Data Minus
3	DP	Data Plus
4	ID	Not used
5	**DGND**	Ground

Table 9: J5 USB type Mini AB connector – FTDI Quad Serial Link

Pin	Name	Comment
1	DIN+	Data In +ve
6	DIN-	Data In -ve
2	SIN+	Strobe In +ve
7	SIN-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT+	Strobe Out +ve
4	SOUT-	Strobe Out -ve
9	DOUT+	Data Out +ve
5	DOUT-	Data Out -ve

Table 10: J2a-J2i SPW-DSU, SPW-0 – SPW-7 interface connections(9x)

Pin	Name	Comment
1	TPFOP	Output +ve
2	TPFON	Output -ve
3	TPFIP	Input +ve
4	TPFOC	Output centre-tap
5		No connect
6	TPFIN	Input -ve
7	TPFIC	Input centre-tap
8		No connect

Table 11: J1A (Top) RJ45 10/100/1000 Mbit/s Ethernet Connector 1

Pin	Name	Comment
1	TPFOP	Output +ve
2	TPFON	Output -ve
3	TPFIP	Input +ve
4	TPFOC	Output centre-tap
5		No connect
6	TPFIN	Input -ve
7	TPFIC	Input centre-tap
8		No connect

Table 12: J1B (Bottom) RJ45 10/100/1000 Mbit/s Ethernet Connector 0

Function	Connector Pin			Function
GPIO0	1	■	2	DGND
GPIO1	3	□	4	DGND
GPIO2	5	□	6	DGND
GPIO3	7	□	8	DGND
GPIO4	9	□	10	DGND
GPIO5	11	□	12	DGND
GPIO6	13	□	14	DGND
GPIO7	15	□	16	DGND
GPIO8	17	□	18	DGND
GPIO9	19	□	20	DGND
GPIO10	21	□	22	DGND
GPIO11	23	□	24	DGND
GPIO12	25	□	26	DGND
GPIO13	27	□	28	DGND
GPIO14	29	□	30	DGND
GPIO15	31	□	32	DGND
(+3.3V)	33	□	34	DGND

Table 13: J4 PIO Header Pin out

Function	Connector Pin			Function
DSUEN	1	■	6	MEM_CLKSEL
BYPASS0	2	□	7	BYPASS1
BYPASS2	3	□	8	IGNLOCK
ETH-CLK	4	□	9	WDOGN
WDRSTN	5	□	10	DGND

Table 14: J5 -Header for Front Panel DIP-Switch

Function	Connector Pin			Function
nc	1	■	2	nc
nc	3	□	4	nc
nc	5	□	6	nc
nc	7	□	8	nc
CTSN-1	9	□	10	RTSN-1
RXD-1	11	□	12	TXD-1
CTSN-0	13	□	14	RTSN-0
RXD-0	15	□	16	TXD-0
+3.3V	17	□	18	+3.3V
DGND	19	□	20	DGND

Table 15: J6– UART - Header for UART Accessory board

Function	Connector Pin			Function
nc	1	■	2	TX-1
RX-1	3	□	4	nc
TX-0	5	□	6	RX-0
nc	7	□	8	nc
nc	9	□	10	nc
nc	11	□	12	nc
nc	13	□	14	nc
nc	15	□	16	nc
+3.3V	17	□	18	+3.3V
DGND	19	□	20	DGND

Table 16: J7– CAN - Header for CAN Accessory board

Function	Connector Pin			Function
nc	1	■	2	nc
nc	3	□	4	nc
RXEN-A	5	□	6	RXEN-B
TXINH-A	7	□	8	TXINH-B
TX-A	9	□	10	TXN-A
RX-A	11	□	12	RXN-A
TX-B	13	□	14	TXN-B
RX-B	15	□	16	RXN-B
+3.3V	17	□	18	+3.3V
DGND	19	□	20	DGND

Table 17: J8– MIL1553 - Header for MIL1553 Accessory board

Function	Connector Pin		Function
DGND	1	120	DGND
+5V	2	119	+5V
DGND	3	118	DGND
-12V	4	117	-12V
DGND	5	116	DGND
+12V	6	115	+12V
DGND	7	114	DGND
D15	8	113	
D7	9	112	
+3.3V	10	111	+3.3V
DGND	11	110	DGND
D14	12	109	
D6	13	108	
D13	14	107	
D5	15	106	
D12	16	105	
D4	17	104	
D11	18	103	
D3	19	102	
+3.3V	20	101	+3.3V
DGND	21	100	DGND
D10	22	99	
D2	23	98	
D9	24	97	
D1	25	96	
D8	26	95	
D0	27	94	
A26	28	93	A27
A24	29	92	A25
+3.3V	30	91	+3.3V
DGND	31	90	DGND
A22	32	89	A23
A20	33	88	A21
A18	34	87	A19
A16	35	86	A17
A14	36	85	A15
A12	37	84	A13
A10	38	83	A11
A8	39	82	A9
+3.3V	40	81	+3.3V
DGND	41	80	DGND
A6	42	79	A7
A4	43	78	A5
A2	44	77	A3
A0	45	76	A1
WRITEN	46	75	
OEN	47	74	IOSN
ROMSN0	48	73	ROMSN1
	49	72	
+3.3V	50	71	+3.3V
DGND	51	70	DGND
	52	69	
	53	68	
	54	67	
	55	66	
	56	65	
	57	64	
BRDYN	58	63	
RESETN	59	62	EXP_CLK
DGND	60	61	DGND

Table 18: Expansion connector J9 Pin-out (see also section 4.5.5)

Function	Connector Pin			Function
SPI_SLVSEL0	1	■ □	6	SPI_CS1
SPI_MOSI	2	□ □	7	SPI_MISO
SPI_SCK	3	□ □	8	SPI_SEL
DGND	4	□ □	9	DGND
+3V3	5	□ □	10	+3V3

Table 19: J10- SPI Header for User SPI interface

Pin	Name	Comment
1	VJTAG	3.3V
2	**DGND**	Ground
3	TCK	JTAG: TCK
4	TDO	JTAG: TDO
5	TDI	JTAG: TDI
6	TMS	JTAG: TMS

Table 20: J11 ASIC – JTAG Connector

Pin	Name	Comment
1	VJTAG	3.3V
2	**DGND**	Ground
3	B-TCK	JTAG: TCK
4	B-TDO	JTAG: TDO
5	B-TDI	JTAG: TDI
6	B-TMS	JTAG: TMS

Table 21: J12 PCI-Bridge – JTAG Connector

Pin	Name	Comment
1	F-TCK	JTAG: TCK
2	DGND	Ground
3	F-TDO	JTAG: TDO
4	nc	no connect
5	F-TMS	JTAG: TMS
6	VREF	3.3V
7	VPUMP	Programming Voltage
8	F-TRSTN	JTAG: TRSTN
9	F-TDI	JTAG: TDI
10	**DGND**	Ground

Table 22: J13 FPGA– JTAG Connector

Pin	Name	Comment
+VE	+5V	Inner Pin, 5V, typically 3 A
-VE	**DGND**	Outer Pin Return

Table 23: J14 POWER – External Power Connector

Pin	Name	Comment
1	+12V	+12V Not used
2	**DGND**	Ground
3	**DGND**	Ground
4	+5V	+5V, typically 3 A

Table 24: J15 POWER – External Power Connector

Function	Connector Pin		Function
DGND	1	2	DGND
nc	3	4	nc
nc	5	6	nc
nc	7	8	nc
nc	9	10	nc
+3.3V	11	12	+3.3V
nc	13	14	nc
nc	15	16	nc
nc	17	18	nc
nc	19	20	nc
DGND	21	22	DGND
pull-up	23	24	pull-up
SD_DQM8	25	26	SD_DQM9
+3.3V	27	28	+3.3V
A0	29	30	A3
A1	31	32	A4
A2	33	34	A5
DGND	35	36	DGND
D71	37	38	D79
D70	39	40	D78
D69	41	42	D77
D68	43	44	D76
+3.3V	45	46	+3.3V
D67	47	48	D75
D66	49	50	D74
D65	51	52	D73
D64	53	54	D72
DGND	55	56	DGND
nc	57	58	nc
nc	59	60	nc
SD_CLK0	61	62	SD_CKE0
+3.3V	63	64	+3.3V
SD_RASN	65	66	SD_CASN
SD_WEN	67	68	SD_CKE1
SD_CSN0	69	70	A12
SD_CSN1	71	72	A13
nc	73	74	SD_CLK1
DGND	75	76	DGND
nc	77	78	nc
nc	79	80	nc
+3.3V	81	82	+3.3V
D23	83	84	D31
D22	85	86	D30
D21	87	88	D29
D20	89	90	D28
DGND	91	92	DGND
D19	93	94	D27
D18	95	96	D26
D17	97	98	D25
D16	99	100	D24
+3.3V	101	102	+3.3V
A6	103	104	A7
A8	105	106	SD_BA0
DGND	107	108	DGND
A9	109	110	SD_BA1
A10	111	112	A11
+3.3V	113	114	+3.3V
SD_DQM2	115	116	SD_DQM3
SD_DQM0	117	118	SD_DQM1
DGND	119	120	DGND
D7	121	122	D15
D6	123	124	D14
D5	125	126	D13
D4	127	128	D12
+3.3V	129	130	+3.3V
D3	131	132	D11
D2	133	134	D10
D1	135	136	D9
D0	137	138	D8
DGND	139	140	DGND
SDSDA0 / pulled high	141	142	SDSCL / pulled high
+3.3V	143	144	+3.3V

Table 25: J16 SODIMM – 144 pin socket for SDRAM SODIMM – bits 31..0 & 79..64

Function	Connector Pin		Function
DGND	1	2	DGND
nc	3	4	nc
nc	5	6	nc
nc	7	8	nc
nc	9	10	nc
+3.3V	11	12	+3.3V
nc	13	14	nc
nc	15	16	nc
nc	17	18	nc
nc	19	20	nc
DGND	21	22	DGND
pull-up	23	24	pull-up
SD_DQM10	25	26	SD_DQM11
+3.3V	27	28	+3.3V
A0	29	30	A3
A1	31	32	A4
A2	33	34	A5
DGND	35	36	DGND
D87	37	38	D95
D86	39	40	D94
D85	41	42	D93
D84	43	44	D92
+3.3V	45	46	+3.3V
D83	47	48	D91
D82	49	50	D90
D81	51	52	D89
D80	53	54	D88
DGND	55	56	DGND
nc	57	58	nc
nc	59	60	nc
SD_CLK2	61	62	SD_CKE0
+3.3V	63	64	+3.3V
SD_RASN	65	66	SD_CASN
SD_WEN	67	68	SD_CKE1
SD_CSN0	69	70	A12
SD_CSN1	71	72	A13
nc	73	74	SD_CLK3
DGND	75	76	DGND
nc	77	78	nc
nc	79	80	nc
+3.3V	81	82	+3.3V
D55	83	84	D63
D54	85	86	D62
D53	87	88	D61
D52	89	90	D60
DGND	91	92	DGND
D51	93	94	D59
D50	95	96	D58
D49	97	98	D57
D48	99	100	D56
+3.3V	101	102	+3.3V
A6	103	104	A7
A8	105	106	SD_BA0
DGND	107	108	DGND
A9	109	110	SD_BA1
A10	111	112	A11
+3.3V	113	114	+3.3V
SD_DQM6	115	116	SD_DQM7
SD_DQM4	117	118	SD_DQM5
DGND	119	120	DGND
D39	121	122	D47
D38	123	124	D46
D37	125	126	D45
D36	127	128	D44
+3.3V	129	130	+3.3V
D35	131	132	D43
D34	133	134	D42
D33	135	136	D41
D32	137	138	D40
DGND	139	140	DGND
SDSDA1 / pulled high	141	142	SDSCL / pulled high
+3.3V	143	144	+3.3V

Table 26: J17 SODIMM – 144 pin socket for SDRAM SODIMM – bits 63..32 & 95..80

6.2 List of Oscillators, Switches and LED's

Name	Function	Description
X1	SPW-CLK	3.3V oscillator in 8 pin DIL format. Nominally 100MHz
X2	MEM-CLK	3.3V oscillator in 8 pin DIL format. Nominally 50 MHz
X3	PCI-CLK	3.3V oscillator in 8 pin DIL format. Nominally 33MHz
X4	SYS-CLK	3.3V oscillator in 8 pin DIL format. Nominally 50MHz
X5	1553-CLK	3.3V oscillator in 5x7mm SMD format. Soldered. Nom 20MHz
Y1	USB-XTAL	USB PHY clock, 12MHz, SMD soldered
Y2	ETH-XTAL	Ethernet PHY clock, 25MHz, SMD soldered
Y3	ETH0-XTAL	Ethernet-0 PHY clock, 25MHz, SMD soldered
Y4	ETH1-XTAL	Ethernet-1 PHY clock, 25MHz, SMD soldered

Table 27: List and definition of Oscillators and Crystals

Name	Function	Description
D1-D16	GPIO	Front panel dual LED's indicating the status of the 16 bit GPIO signals.
D17	POWER	3.3V power
D18	PLL0 / PCIMODE	Front panel dual LED's indicating PLL0 / PCIMODE (bottom/top)
D19	PLL1 / MEMWIDTH	Front panel dual LED's indicating PLL1 / MEMWIDTH
D20	PLL2 / DSU Active	Front panel dual LED's indicating PLL2 / DSU Active
D21	PLL3 / ERRORN	Front panel dual LED's indicating PLL3 / ERRORN
D22	PLL4 / WATCHDOG	Front panel dual LED's indicating PLL4 / WATCHDOG
D23	PLL5 / SYSLOCK	Front panel dual LED's indicating PLL5 / 'STATUS'
D24	PROM-BUSY	Illuminated when Flash PROM is being written or erased.

Table 28: List and definition of PCB mounted LED's

Name	Function	Description
S1	BREAK	Toggle (on/off) BREAK switch
S2	RESET	Push button RESET switch
FP-S1	GPI0[7..0]	8 pole SPDT DIP switch: Pull-up/Float/Pull-Down
FP-S2	GPIO[15..8]	8 pole SPDT DIP switch: Pull-up/Float/Pull-Down
FP-S3	CONFIG	8 pole DIP switch (Logic '1' when 'open'): See table below

Table 29: List and definition of Switches

Function	Open ('1')	Switch	Closed ('0')
DSUEN	ENABLE	1	DISABLE
MEM_CLKSEL	Clk Source= X2	2	Clk Source=X1
BYPASS0	PLL0 Bypassed	3	PLL0 operational
BYPASS1	PLL1 Bypassed	4	PLL1 operational
BYPASS2	PLL2 Bypassed	5	PLL2 operational
IGN	Ignore PLL lock	6	Enable PLL lock
ETH-CLK	GBit	7	100Mbit
WDOGN	WDOG disconnect	8	WDOG connect

Table 30: DIP Switch FP-S3 definition

6.3 List of Jumpers

Name	Function	Type	Description
JP1	FP-Switch	2x2 pin 0.1” Hdr	Header for front panel RESET and BREAK switches
JP2	UART1-FTDI	4x2 pin 0.1” Hdr	Jumpers to connect UART1 to FTDI chip
JP3	UART0-FTDI	4x2 pin 0.1” Hdr	Jumpers to connect UART0 to FTDI chip
JP4	JTAG-FTDI	4x2 pin 0.1” Hdr	Jumpers to connect ASIC-JTAG to FTDI chip
JP5	PM-I2C-FTDI	3x2 pin 0.1” Hdr	Jumpers to connect Power Measure I2C to FTDI chip
JP6	Flash-CONF	6x2 pin 0.1” Hdr	Jumpers to Configure flash address and Write-Protection
JP7	GPIO[7..4]	4x2 pin 0.1” Hdr	Jumpers to connect GPIO[7..4] to SPW-DSU
JP8	SPI-OB	2 pin 0.1” Hdr	Jumper to connect on-board AD7814 chip as SPI peri.
JP9	VC0-CLKSEL	2 pin 0.1” Hdr	Jumper for CLKSEL of Ethernet I/F Versaclock
JP10	VC0-PROG	2 pin 0.1” Hdr	Jumper for Programming mode of Eth. I/F Versaclock
JP11	PROMIO/IF	22x4 pin 0.1” Hdr	Jumpers to connect pins as PROM or I/F functions
JP12	+3.3V	2 pin 0.1” Hdr	Test/Power header (Pin 1 = DGND, Pin2 = +3.3V)
JP13	+VIN	2 pin 0.1” Hdr	Test/Power header (Pin 1 = DGND, Pin2 = +5V)
JP14	I3V3asic	2 pin 0.1” Hdr	Test point for 3.3V current (Link normally installed)
JP15	I2V5	2 pin 0.1” Hdr	Test point for 2.5V current (Link normally installed)
JP16	I1V2	2 pin 0.1” Hdr	Test point for 1.2V current (Link normally installed)
JP17	TESTEN	2 pin 0.1” Hdr	Install to set ASIC test Mode (no user function)
JP18	PCI66	2 pin 0.1” Hdr	Insert jumper for 66MHz capability. Default: 33MHz
JP19	PCI_RSTN	2 pin 0.1” Hdr	Connects board RESETN to PCI_RSTN for Host mode 2-3: PCI reset => board reset 1-2: Board reset => PCI reset
JP20	VC1-CLKSEL	2 pin 0.1” Hdr	Jumper for CLKSEL of SDRAM I/F Versaclock
JP21	VC1-PROG	2 pin 0.1” Hdr	Jumper for Prog. mode of SDRAM I/F Versaclock
JP22	BP-CLK	2 pin 0.1” Hdr	Remove to stop board driving PCI backplane clocks
JP23	M66EN	2 pin 0.1” Hdr	Install to pull M66EN low, and force backplane to operate with 33MHz speed.
JP24	FPGA-CFG	3x2 pin 0.1” Hdr	Configuration jumpers for FPGA: see Table 3

Table 31: List and definition of PCB Jumpers

(for details refer to schematic, [RD2])

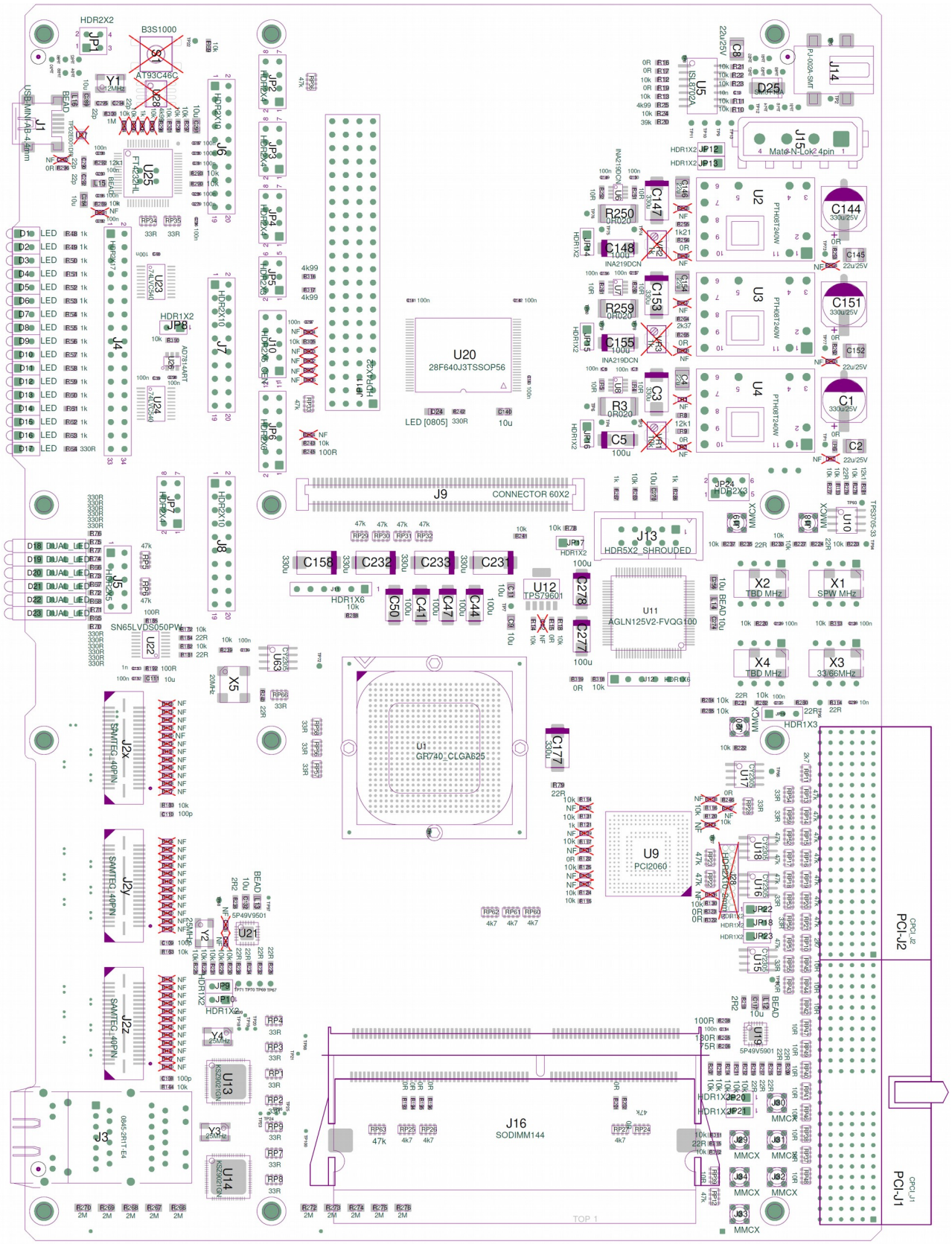


Figure 6-2: PCB Top View

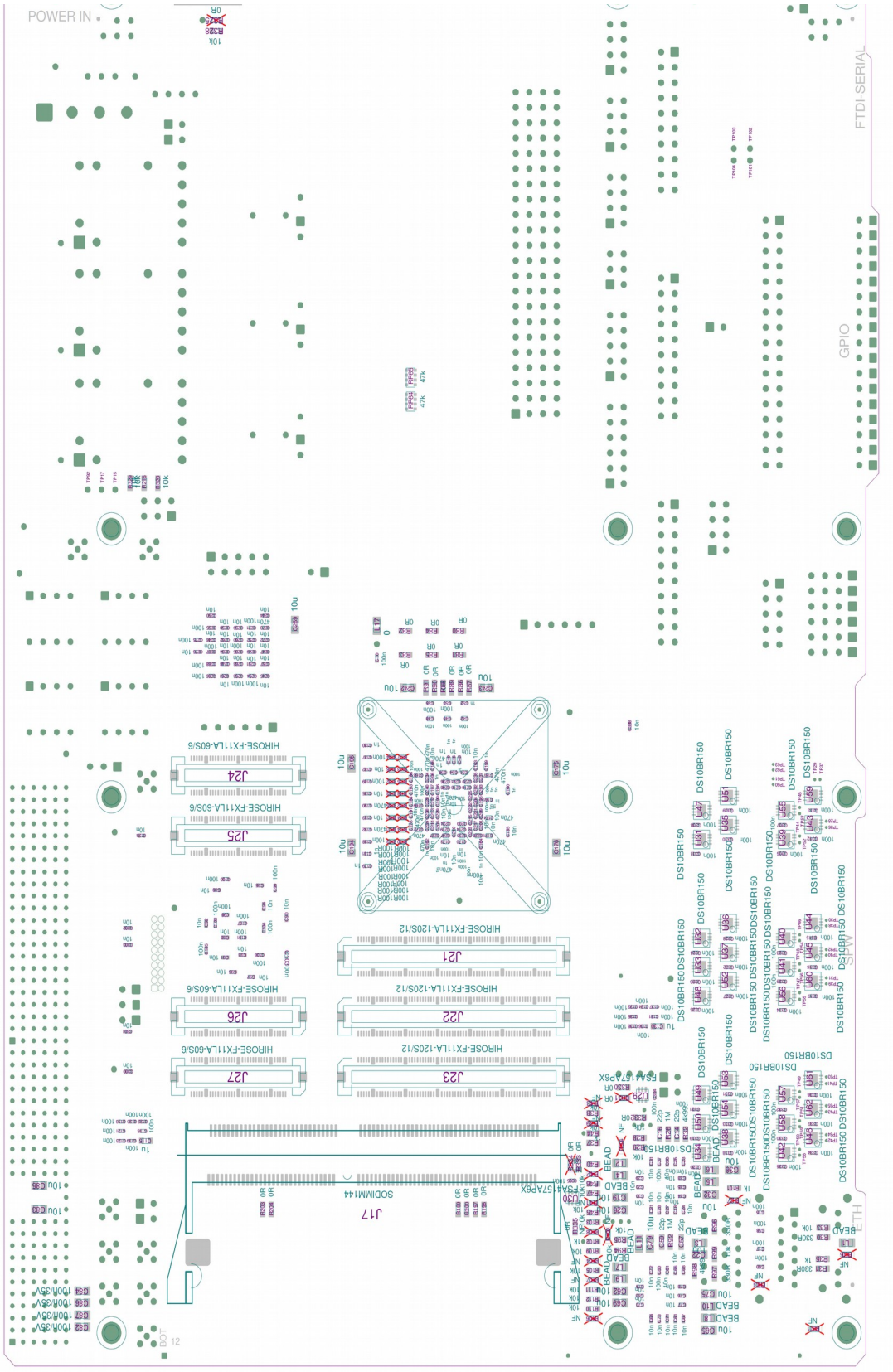


Figure 6-3: PCB Bottom View

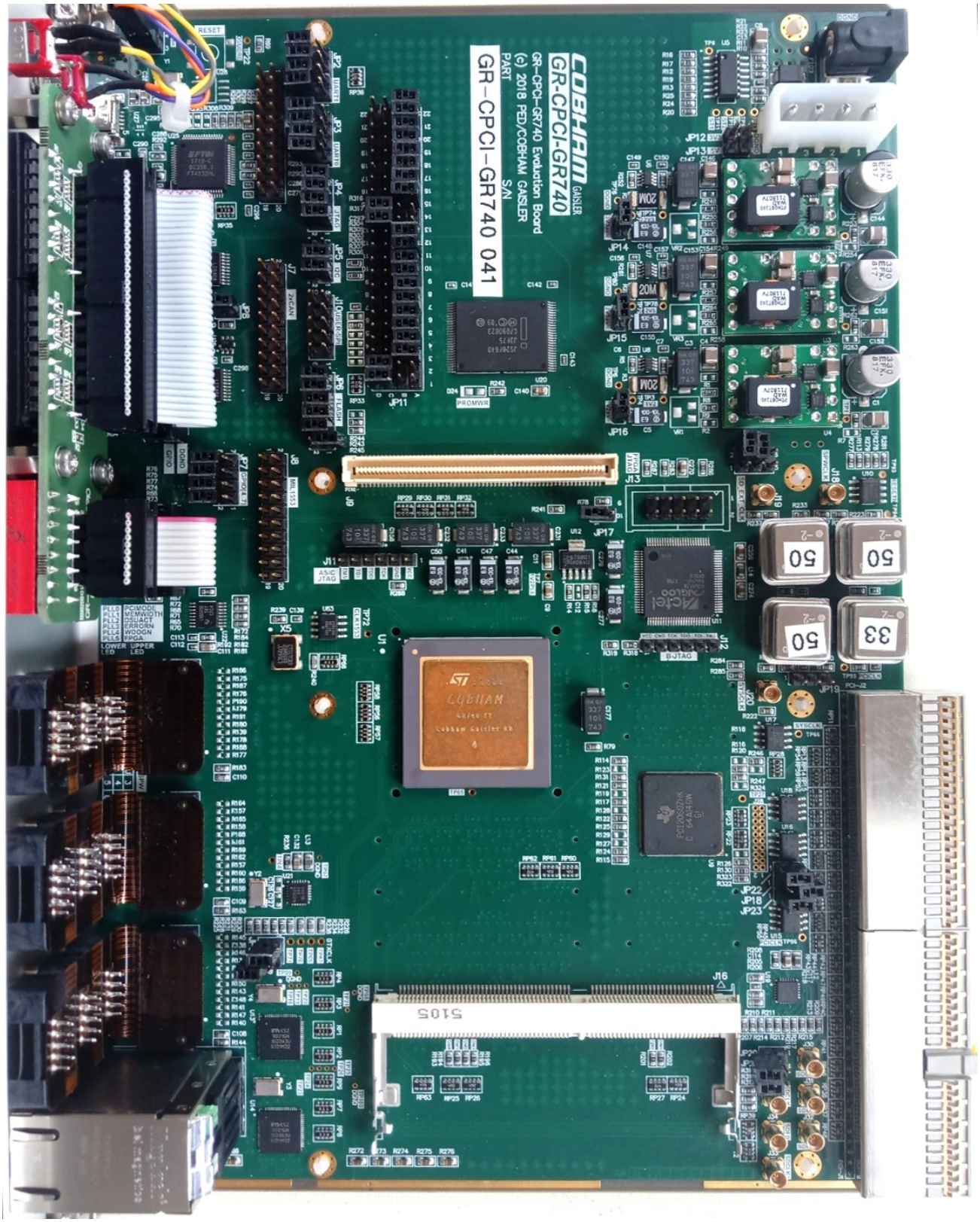


Figure 6-4: PCB Top View (Photo)

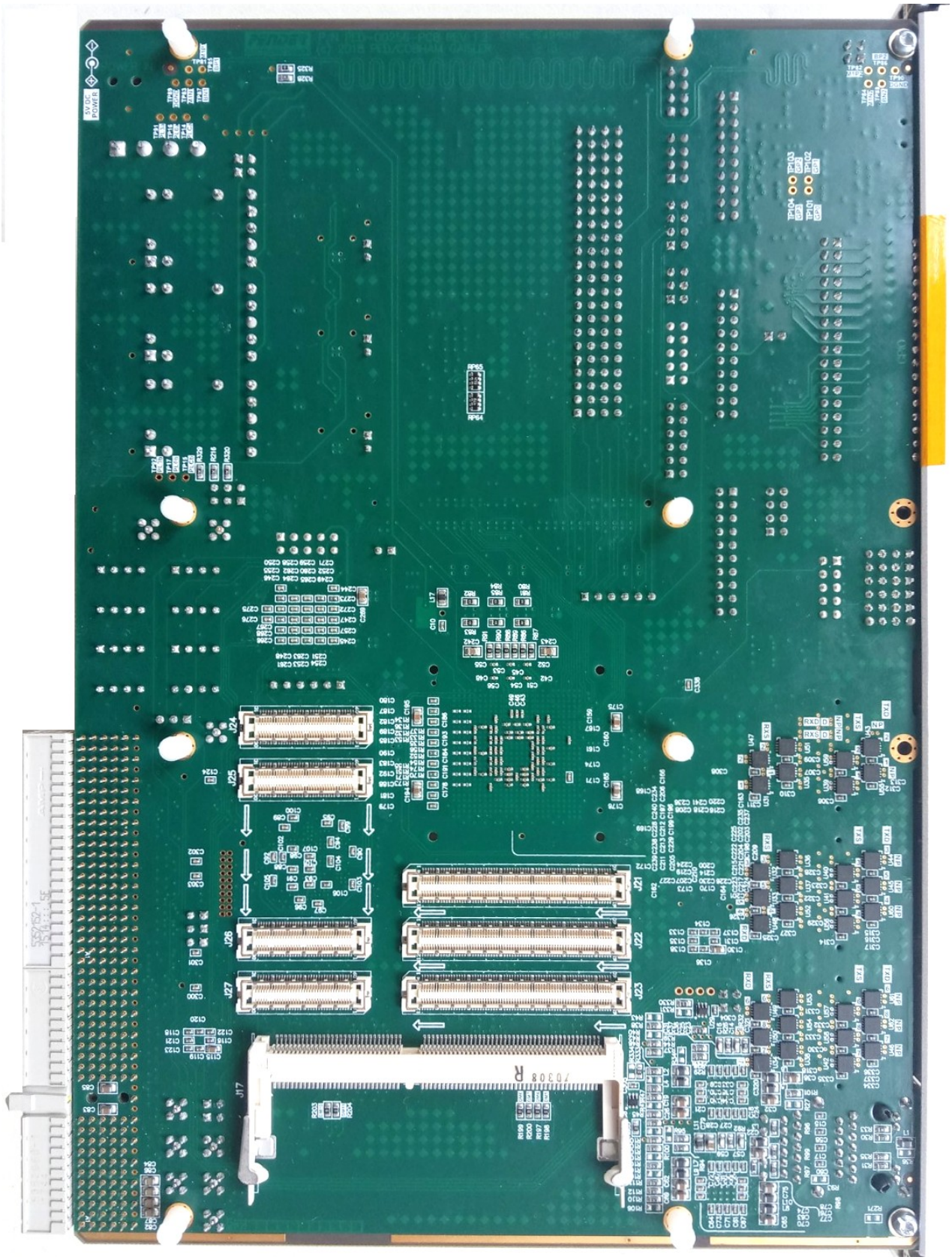


Figure 6-5: PCB Bottom View (Photo)

7 Change Record

Issue	Date	Section / Page	Description
0.0	2015-10-12	All	Draft Issue
0.1	2016-01-23	All	Draft Issue. New Frontgrade Gaisler template
1.1	2016-02-26	All	Updated after prototype hardware
1.2	2016-06-01	§4.7 §4.17 & 4.18 Table 6 Table 7 Figure 6-2& Figure 6-3 General	Added note concerning shared MDIO bus. Removed since not relevant for rev 1.1 of the board. Corrected jumper setting for JP11 Corrected default DIP switch settings Updated to rev 1.1 of Assembly Drawing Update of figures and drawings
1.3	2016-09-26	§4.5.3	Added Table 1 with individual JP11 pin configuration.
1.4	2017-01-11	§4.16.2 §4.16.5 §4.7	Corrected typo in connectors J14, J15 Corrected typo in connector J11 Corrected typo in oscillator Y2
1.5	2017-06-09		
1.6	2017-06-29		
1.7	2017-09-11	§4.5.2 §4.5.3 §4.11 §6.3 and 4.6.6	Fix typo: change 48 bit to 96 bit in fourth paragraph Add note about floating address lines Corrected text and block diagram for SPI interface Update and correct information on JP19 and PCI reset
1.8	2018-04-19	General §4.5.3 Table 8 Table 24 Figure 4-3 Figure 4-5 Figure 6-2 & Figure 6-3	Updated to reflect hardware rev.1.2 status. Added additional note about pull-down resistors in rev 1.2 board. Header changed from 22x3 pin to 22x4 pin configuration Added new test connectors to list of connectors Corrected pin out for connector J15 Indicate re-driver circuits in Block Diagram Update photo of GR740-BOX system Updated for Rev 1.2 PCB layout
1.9	2018-11-01	1.1 - 4.13 4.16.1 Table 7 Table 27 Table 23 & Table 24 Figure 6-4 & Figure 6-5 Figure 4-31	Add board version information. GRMON2 → GRMON3 Updated MEM_CLKSEL dip switch configuration. Updated oscillator specification for memory clock. Updated default configuration for FP-S1-7 & 8. Updated X2 value. Updated specification for external power connector. Updated latest photos. Updated oscillator values.
2.0	2019-03-28	Figure 4-11 1.2 4.6 Figure 4-30 4.16.1 & 7 Table 22	Fixed numbering. Updated reference document locations. Fixed incorrect reference to figure. Updated figure. Fixed broken reference. Fixed table formatting.
2.1	2019-04-24	5	Fixed wrong configuration information for DIP switch

2.2	2019-05-07	4.9.3	Included precautions to be taken during SPW port connection.
2.3	2019-05-27	4.5.3	Fixed wrong configuration for full PROM/IO mode
2.4	2025-11-06	- Figure 4-4 Figure 4-2 Figure 4-1 3.1,4.1 4.10 3.2 1.1	Updated company name Updated board photo Updated Device package photo Updated SoC block diagram Clarification about packaging Added pin multiplexing reference Updated ESD warning Fixed broken links

Frontgrade Gaisler AB
Kungsgatan 12
411 19 Göteborg
Sweden
www.gaisler.com
sales@gaisler.com
T: +46 31 7758650
F: +46 31 421407