FRONTGRADE Gaisler

Board User's Manual

GR716B Board User's Manual

May 2026, Version 1.1

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1 INTRODUCTION

1.1 Scope and Purpose of the Document

This document provides a User's Manual and Interface document for the “GR716B-BOARD” Development and Demonstration board within the activity “GR716B” initiated by the European Space Agency under ESTEC contract 4000130767/20/NL/MM/gm.

The work has been performed by Frontgrade Gaisler AB, Göteborg, Sweden.

1.2 Reference Documents

[RD1] GR716B, Advanced Data Sheet and User's Manual, Frontgrade Gaisler, GR716B-UM, GR716B-CQFP-DS, available from
https://www.gaisler.com/index.php/products/components/gr716/gr716b

[RD2] GR716B-BOARD_schematic.pdf, Schematic

[RD3] GR716B-BOARD_assy_drawing.pdf, Assembly Drawing

[RD4] GRMON User's Manual, available from:
https://www.gaisler.com/index.php/products/debug-tools/grmon4

2 ABBREVIATIONS

ADC	Analog to Digital Converter
ASIC	Application Specific Integrated Circuit.
CPCI	Compact Peripheral Component Interconnect
DAC	Digital to Analog Converter
DSU	Debug Support Unit
EDAC	Error Detection and Correction
ESA	European Space Agency
ESD	Electro-Static Discharge
ESTEC	European Space Research and Technology Center
GPIO	General Purpose Input / Output
IC	Integrated Circuit
I/O	Input/Output
IP	Intellectual Property
LDO	Low Drop-Out
LVDS	Low-voltage differential Signalling
PCB	Printed Circuit Board
POL	Point of Load
SOC	System On a Chip
SPW	SpaceWire

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3 INTRODUCTION

3.1 Overview

This document describes the GR716B-BOARD Development Board as shown in Figure 3-1.

This equipment is intended to be used as a platform for the demonstration of the Frontgrade Gaisler GR716B RAD Hard Microcontroller.

Furthermore, this board provides developers with a convenient hardware platform for the evaluation and development of software for the GR716B microcontroller.

The GR716B Microcontroller features a fault-tolerant LEON3FT SPARC V8 processor, communication interfaces and on-chip ADC, DAC, Power-on-Reset, Oscillator, Brown-out detection, LVDS transceivers, regulators to support for single 3.3V supply, ideally suited for space and other high-rel applications.

The GR716B Microcontroller is a complex device with multifunctional pins whose function depend on the mode of operation and programming of internal registers of the device. This board treats the pins in a generic manner to allow easy access to all the pins and features of the GR716B microcontroller.

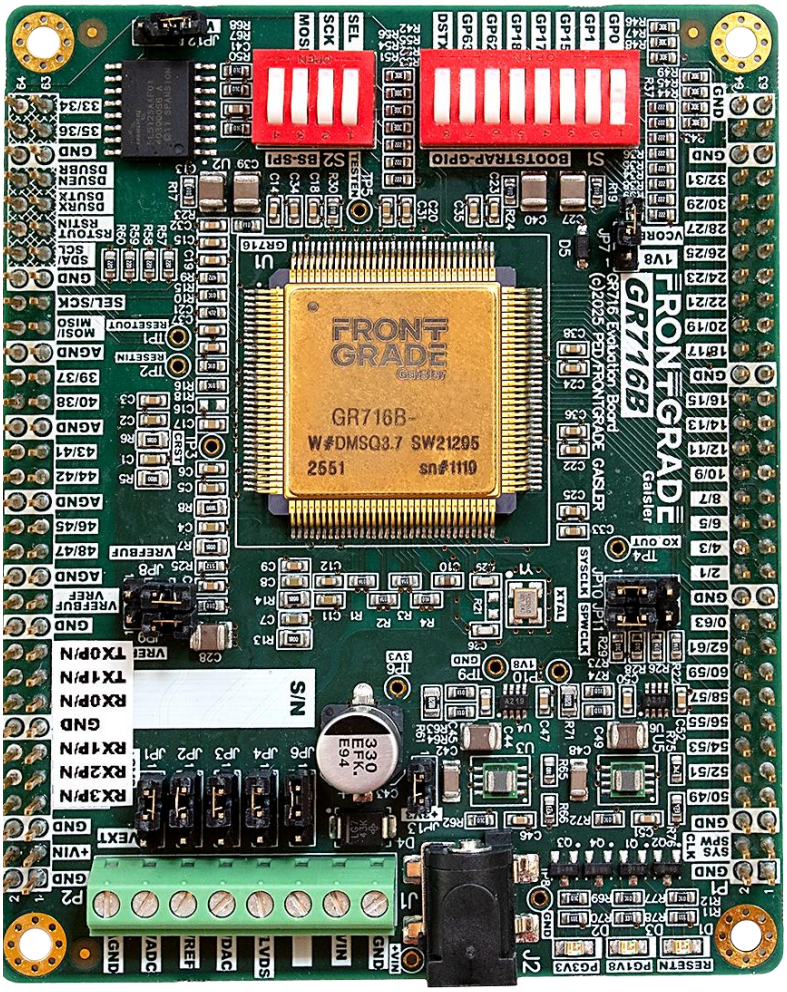

Figure 3-1 GR716B-BOARD Development Board

The board contains the following main items as detailed in section 4 of this document:

- size 80 x 100mm
- two 2x32 pin stackable 0.1” headers allowing access to all I/O pins
- connector for single VIN power input (+5V min, +12V nom, 14.5 max)
- alternative connector for connections to individual device power supplies
- jumpers for power supply configuration
- on-board regulators converting from VIN to 3.3V & 1.8V
- 512 Mbit SPI memory (Infineon, S25FL512SAGM in 16 pin SOIC package)
- crystal 20 MHz
- DIP switch for bootstrap settings
- on-board I2C voltage/current measurement

3.2 Handling

ATTENTION: OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES

This unit contains sensitive electronic components which can be damaged by Electrostatic Discharges (ESD). When handling or installing the unit observe appropriate precautions and ESD safe practices.

When not in use, store the unit in an electrostatic protective container or bag.

When configuring the jumpers on the board, or connecting/disconnecting cables, ensure that the unit is in an un-powered state.

When operating the board in a 'stand-alone' configuration, the power supply should be current limited to prevent damage to the board or power supply in the event of an over-current situation.

This board is intended for commercial use and evaluation in a standard laboratory environment, nominally, 20°C. All devices are standard commercial types (except the microcontroller), intended for use over the standard commercial operating temperature range (0 to 70ºC).

4 BOARD DESIGN

4.1 Board Block Diagram

The GR716B-BOARD Board provides the electrical functions and interfaces as represented in the block diagram, Figure 4-2.

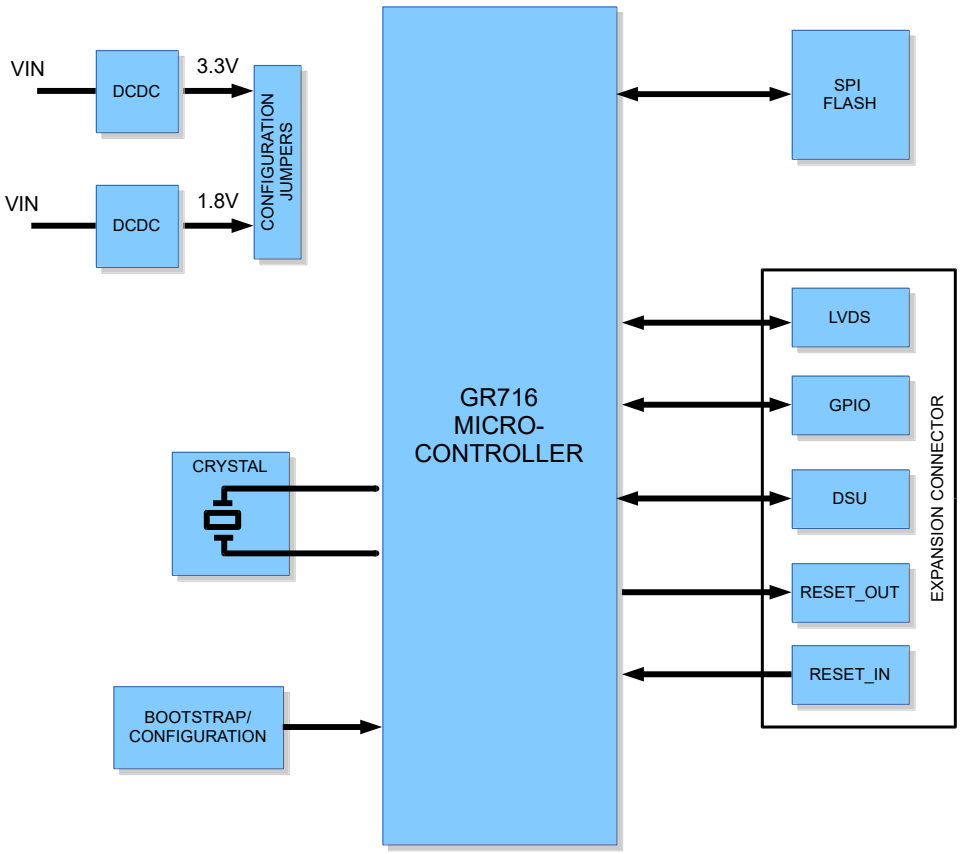

Figure 4-1 GR716B-BOARD Board Block Diagram

Note that not all features and interfaces are available at the same time, and the configuration of on-board resistors plus programming of registers is required to access some of the features.

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4.2 Board Mechanical Configuration

The board (80 x 100mm) and can be used 'stand-alone' on the bench-top simply an external +5V power supply connected to connector J2. For mounting of the board on a carrier or expansion board, four M2.5 mounting holes are provided in the corners of the board, as shown in the figure below.

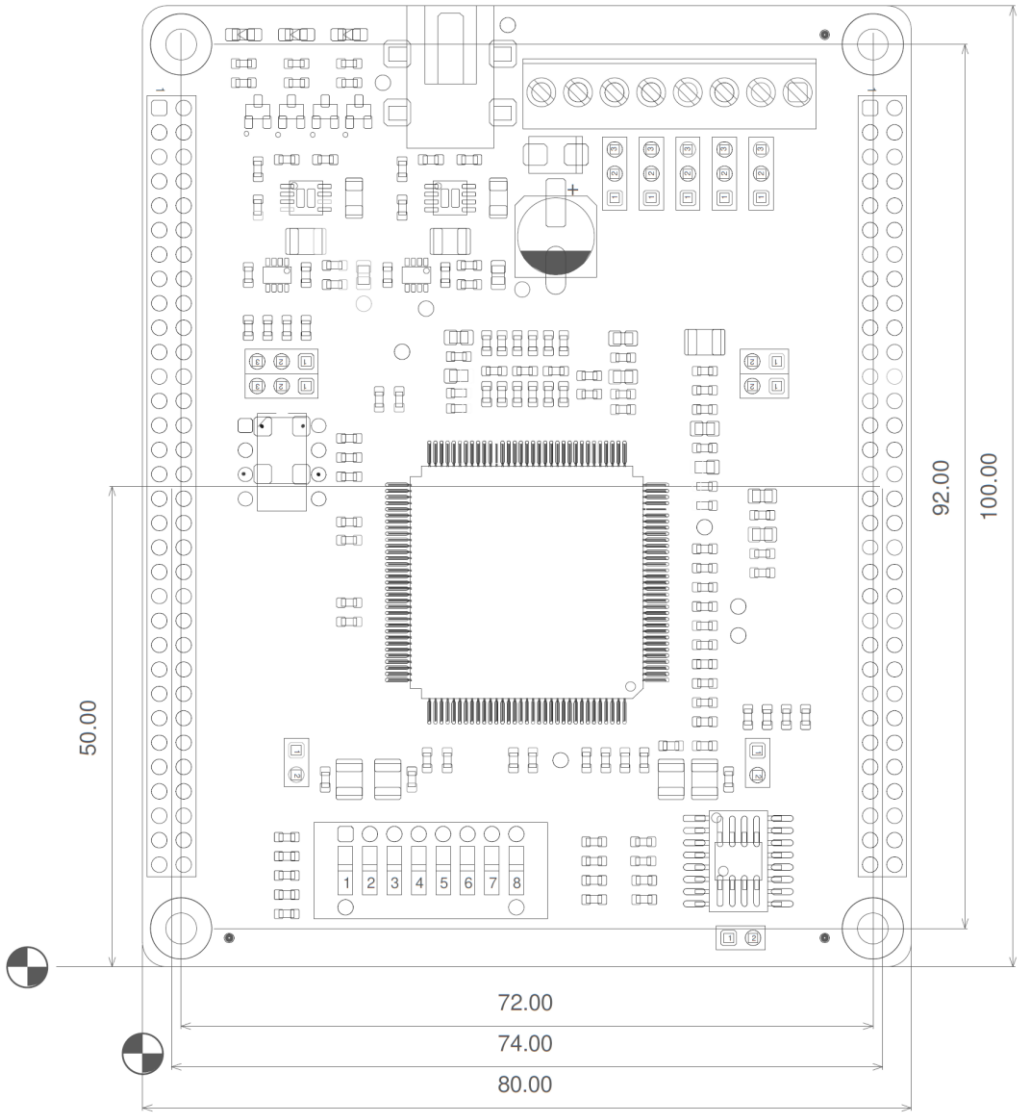

Figure 4-2 GR716B-BOARD Board Dimensions

The expansion connectors P1 and P2 of the GR716B-BOARD are stacking style connectors having a socket on the bottom side and an extended pin on the top side. In a stand-alone configuration the pins on the top side allow easy access for Logic Analyser or Oscilloscope probing for all the functional microcontroller pins.

The sockets on the bottom side allow the board to be plugged on to a carrier board to conveniently enable further development testing.

The CPCI format board providing GPIO, SPW, Serial (via FTDI-USB) and analog coaxial connector which has been developed for this purpose is shown in Figure 4-3.

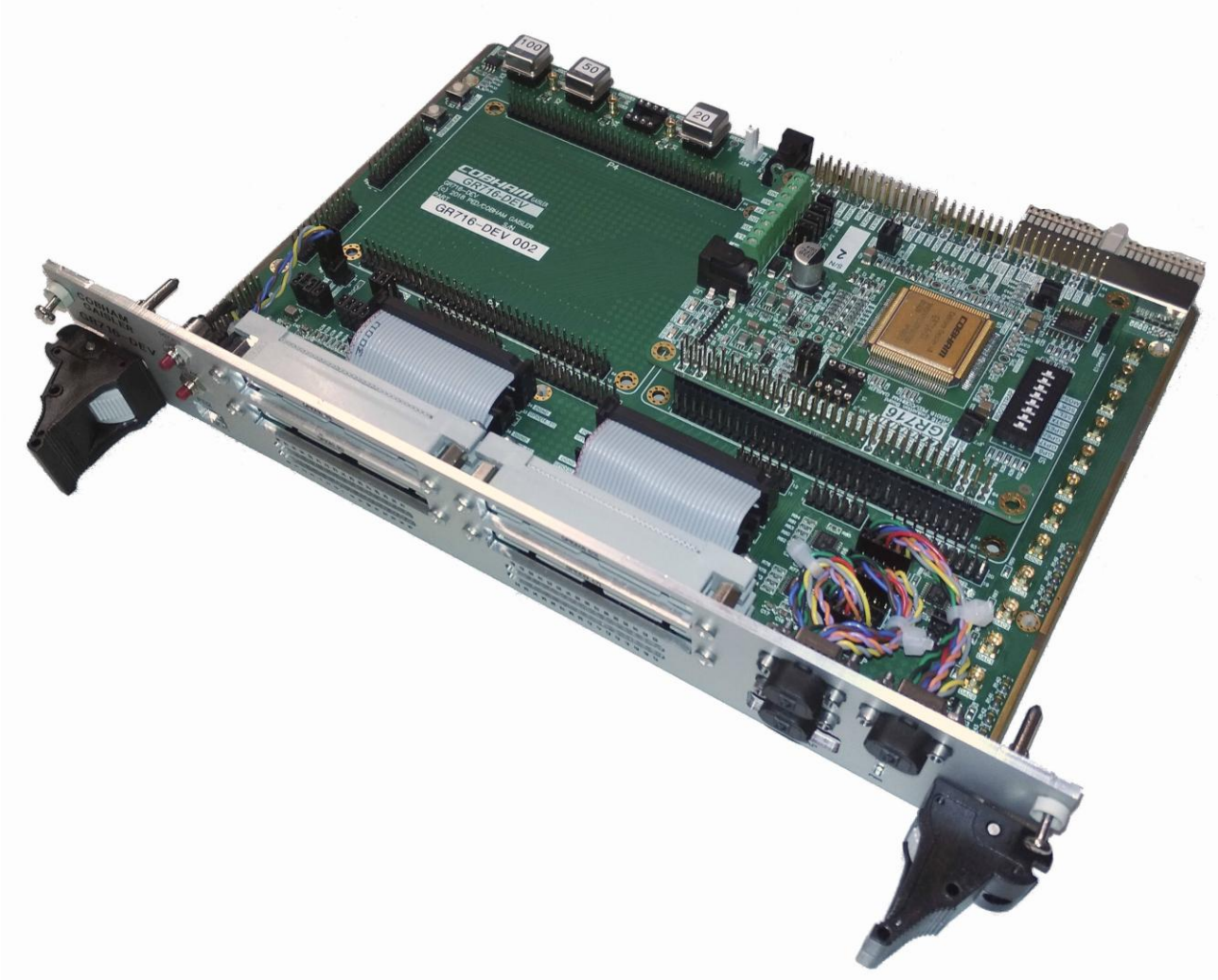

Figure 4-3 GR716B-BOARD mounted on a GR716-CPCI-DEV Carrier board

Alternatively, the stacking connector concept allows the interface functions to be expanded by stacking the GR716B-BOARD to other boards in a concept like PC104.

A test board for adding memory (SPI serial, 8-bit parallel FLASH and 8-bit SRAM) is shown in Figure 4-4.

This concept also provides a convenient way for User Defined interface boards to be developed and connected to the GR716B-BOARD, if other functions or features are to be demonstrated.

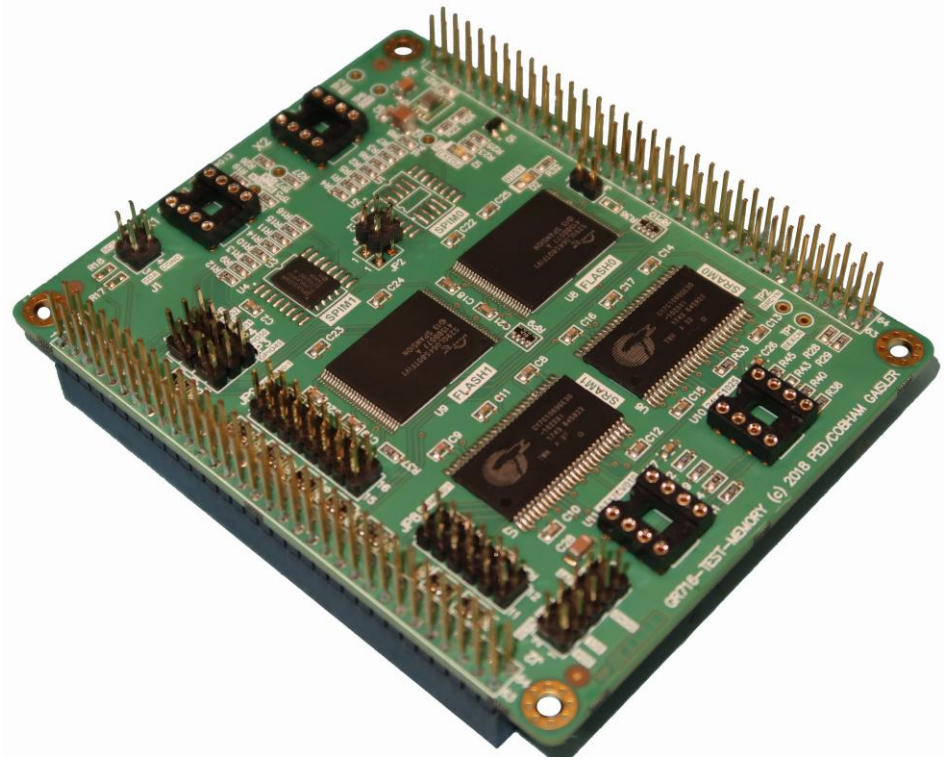

Figure 4-4 GR716-TEST-MEMORY BOARD

4.3 GR716B Microcontroller

The *Frontgrade Gaisler GR716B Microcontroller* features a fault-tolerant LEON3FT SPARC V8 processor, communication interfaces and on-chip ADC, DAC, Power-on-Reset, Oscillator, Brown-out detection, LVDS transceivers, regulators to support for single 3.3V supply, ideally suited for space and other high-rel applications.

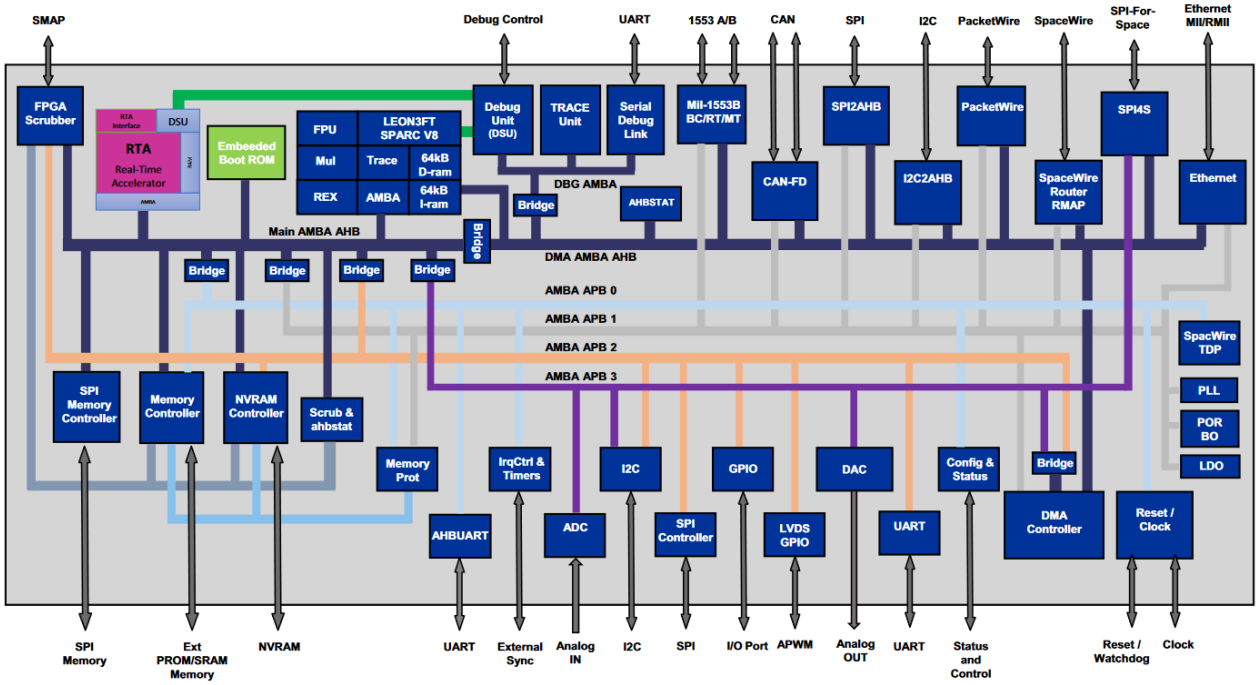

Figure 4-5 GR716B Microcontroller Block Diagram

The GR716B Microcontroller is a complex device with many modes of operation. For the details of the interfaces, operation and programming, refer to [RD1].

The GR716B microcontroller is packaged in a 132-pin, 0.635mm pitch Ceramic Quad Flat Pack package (housing: 24 x 24 mm).

Figure 4-6 GR716B Package

4.4 Memory

The memory configuration installed on the board comprises:

- 512 Mbit SPI memory (Infineon, S25FL512SAGM in 16 pin SOIC package)

The SPI boot memory is connected directly to the SPIM interface of the GR716B Micro-controller. The SPI memory is interfaced with the GR716B using x1 data mode (GR716B only supports x1 data mode).

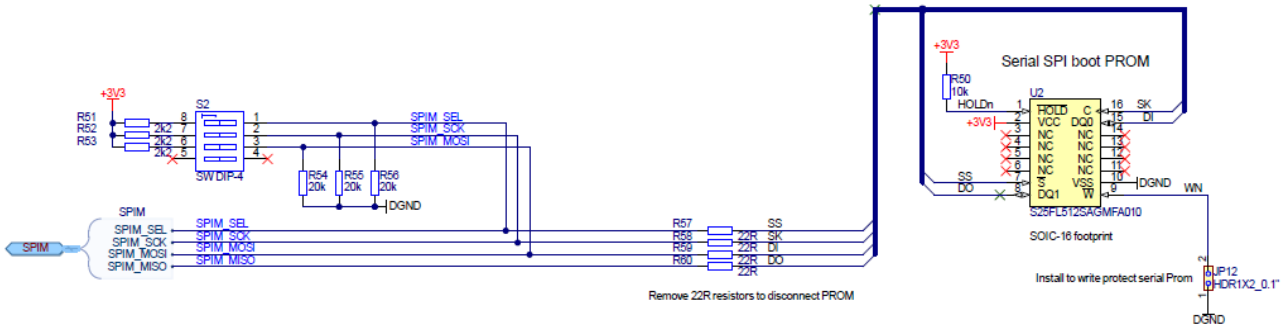

Figure 4-7 SPI Boot Memory Connectors

4.5 LVDS Interfaces

The GR716B microcontroller provides a set of four LVDS input and output pairs which are configurable from software via configuration registers to provide SpaceWire or SPI4SPACE interfaces.

These signals are connected from the GR716B microcontroller to the Expansion connector, P2.

100 Ohm Termination resistors are mounted on the board close to the receiver.

This equipment has SPW ports that use Low Voltage Differential Signalling (LVDS) which has limited common mode voltage protection. To avoid damage to the SPW interfaces due to common mode voltage the following actions should be performed before the equipment's that will be connected by SpaceWire are powered on.

- Before connecting any SpaceWire cables, make sure that there is no voltage difference between the different equipment grounds. E.g., measure the voltage between the different equipment grounds with a voltmeter. The result should be close to 0 V.
- After the SpaceWire cables are connected, make sure that the equipment grounds are low ohmic connected to each other. E.g., measure the resistance between the different equipment grounds with a multimeter in resistance mode. The result should be less than 1 Ω.

This board is intended to be used together with a carrier board. See the user's manual of the carrier board for information about the connection and grounding of the SpaceWire interface. Users using the board stand alone or design their own carrier board, must ensure that equipment's connected via SPW have grounds that are connected together.

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4.6 GPIO

All 64 GPIO pins are connected from the GR716B Microcontroller to the Expansion connector.

These General purpose I/O pins are 3.3V LVCMOS voltage levels.

Note though that most pins have multiple functions and in certain configurations may have different Input/Output voltage requirements (e.g. ADC and DAC signals). Care must be taken to account for this.

No current limiting or overvoltage protection components are included on the GPIO signals of the GR716B-BOARD board. The signals are connected directly from the microcontroller to the expansion connector. Care must therefore be taken to ensure that any external circuitry connected does not exceed the allowable voltage limits for the Input/Output pins.

4.7 Bootstrap Signals

A number of features of the GR716B microcontroller are required to be set at power-on of the processor, by means of bootstrap pins. A number of GPIO and function pins are pre-defined for this purpose, refer section 3.1 Bootstrap signals of [RD1].

To define the desired setting, an 8 pole, DIP switch (S1) and a 4 pole, DIP switch (S2), is provided on the board to connect these signals to either a pull-up or a pull-down resistor, or to allow the pin to float.

Table 1: Bootstrap Resistor Settings

Switch	Pin	Function	Default
S1-1	GPIO0	Disable EDAC	Up
S1-2	GPIO1	CAN-FD bus Primary or Redundant	Down
S1-3	GPIO15	CAN-FD/I2C node ID [2]	Down
S1-4	GPIO17	Bypass internal Boot PROM	Down
S1-5	GPIO18	CAN-FD remote boot	Down
S1-6	GPIO62	CAN-FD/I2C node ID [1]	Down
S1-7	GPIO63	Redundant Memory Available/SPW default frequency	Down
S1-8	DSUTX	Copy ASW image/SPW default frequency	Down
S2-1	SPIM-SEL	Boot Source 0	Down
S2-2	SPIM_SCK	Boot Source 1	Down
S2-3	SPIM_MOSI	Remote Access/Boot from Memory	Down
S2-4	-	Reserved, not used	-

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4.8 Debug Support Unit Interfaces

Program download and debugging to the processor is performed using the GRMON Debug Monitor tool from Frontgrade Gaisler ([RD4]). The GR716B microcontroller provides a UART based DSU interface for Debug and control of the processor by means of a host terminal, as represented in Figure 4-8.

Four control signals from the Debug Support Unit interface to the processor are implemented:

DSUTX	Debug UART Transmit
DSURX	Debug UART Receive
DSUEN	This signal is pulled high on the board to enable Debugging
DSUBRE	This signal is pulled low on the board

To connect to a host computer, a small adapter can be used as shown in Figure 4-9.

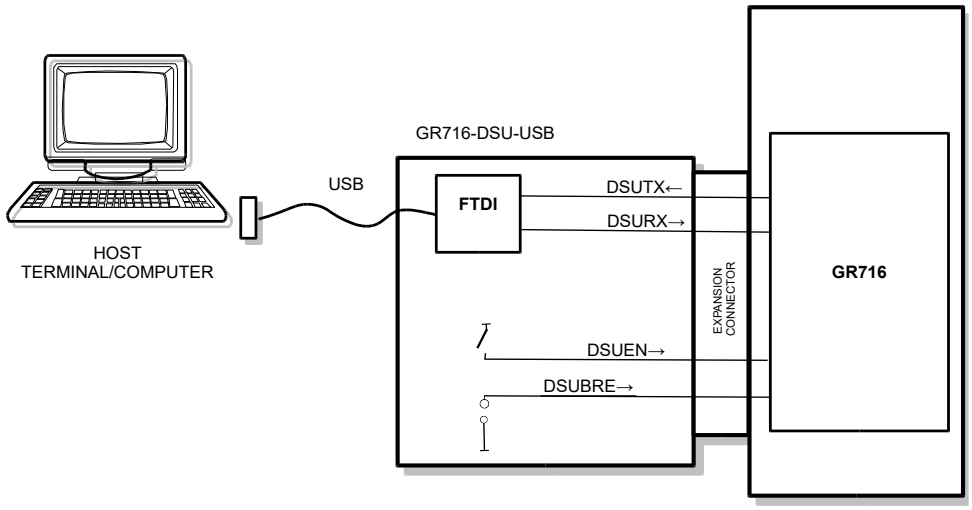

Figure 4-8 Debug Support Unit connections

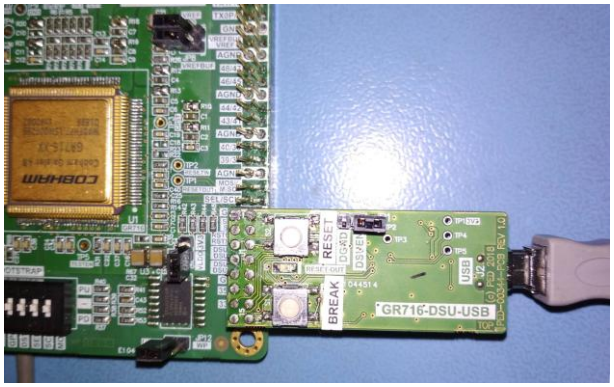

Figure 4-9 GR716-DSU-USB Adapter

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4.9 Oscillators and Clock Inputs

The oscillator and clock scheme for the GR716B-BOARD Board is shown in Figure 4-10.

Two oscillator inputs are required: CLK for the main system clock, and SPW_CLK for the SpaceWire clock of the microcontroller

To allow the GR716B Microcontroller to operate in a standalone manner a crystal is required on the board which is connected to the Crystal oscillator interface (XO_1 and XO_2) for the GR716B. On this board a 20 MHz crystal is connected to this interface.

This generates an output clock, XO_OUT, which is connected to the CLK and SPW_CLK inputs with jumpers.

In an alternative scenario, it may be preferred to have a separate CLK or SYS_CLK to allow different frequencies to be used. In this case the jumpers can be moved and instead an external 3.3V LVCMOS clock signal provided via the expansion connector.

For more details of the internal Crystal Oscillator, PLL structure and clock gating features of the GR716B, please refer to sections 9 and 10 of [RD1].

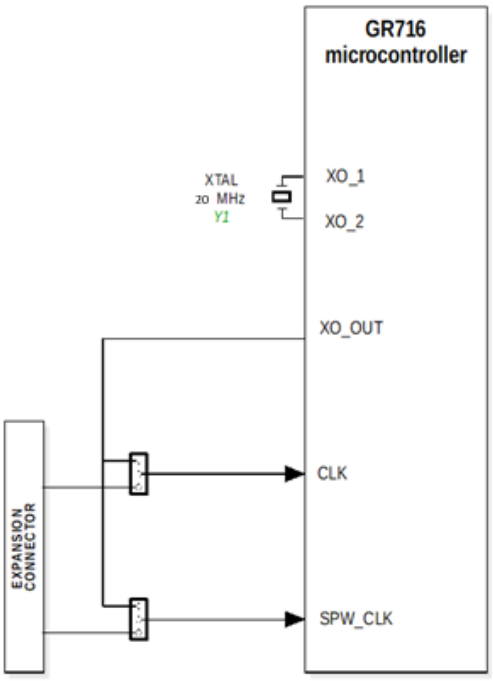

Figure 4-10 Board level Clock Distribution Scheme

4.10 Power Supply and Voltage Regulation

The power configuration is represented in Figure 4-11.

By means of configuration jumpers, several configurations can be tested:

1. Individual voltages from external bench supplies connected to the screw terminal connector J1 to provide

   +VADC (+3V3 nominal)

   +VREF (+3V3 nominal)

   +VDAC (+3V3 nominal)

   +VLVDS (+3V3 nominal)

   This allows individual power supplies to be tested over min/nom/max by varying the supply voltages.
2. Single VIN (+12V nominal) input supply connector to J1.
3. Single VIN (+12V nominal) input supply connector to J2.
4. VIN provided from external circuitry connected to Expansion connector P2.

With reference to the setting of the jumpers shown in Figure 4-12:

- In case 1, jumpers JP1, JP2, JP3 and JP4 should be set to position 2-3.
- In cases 2,3,4 VIN is regulated with two LMZ21701 micro Point-of-Load regulators to generate a regulated VDDIO (+3.3V) and VDD_CORE (+1.8V). In these cases, jumpers JP1, JP2, JP3 and JP4 should be set to position 1-2.
- If the GR716B is to be operated from a single 3.3V, and the internal LDO is to be used to generate the VDDCORE voltage of 1.8V then JP6 should be set to position 1-2 and JP7 removed.
- If the GR716B is to be operated from both the POL generated 3.3V and 1.8V supplies, then JP6 should be set to position 2-3 and JP7 installed. In this situation, the internal LDO is disabled and VDDCORE voltage of 1.8V is provided from the POL regulator.

At the output of the 3.3V and 1.8V POL regulators, 20 mOhm sense resistors and INA219 Current/Power Monitor circuits with an I2C interface are incorporated on the board. The I2C signals (SDA, SCL) are connected to the Expansion connector P2 to allow the current/voltage to be measured using an I2C master circuit.

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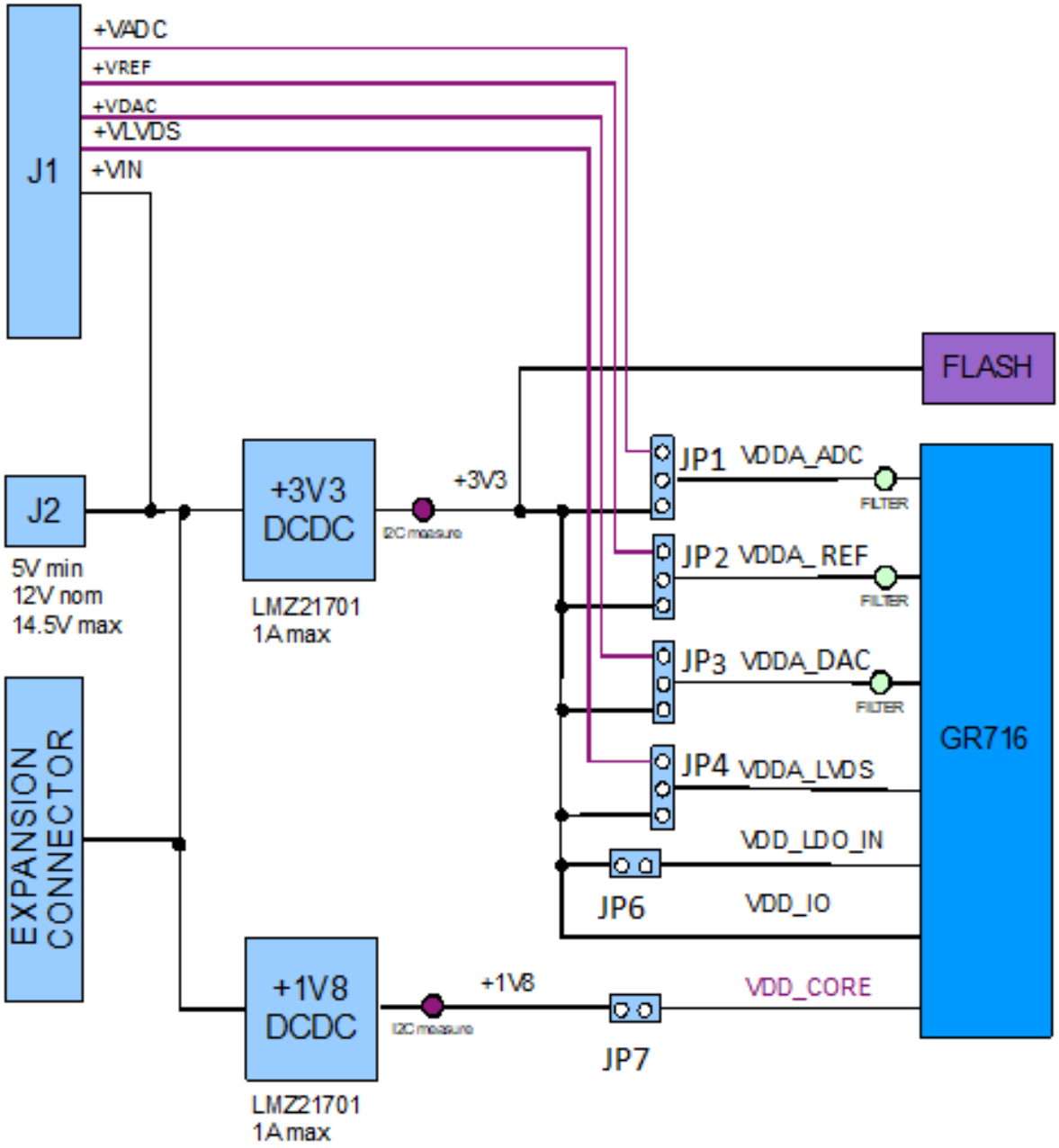

Figure 4-11 Power Regulation Scheme

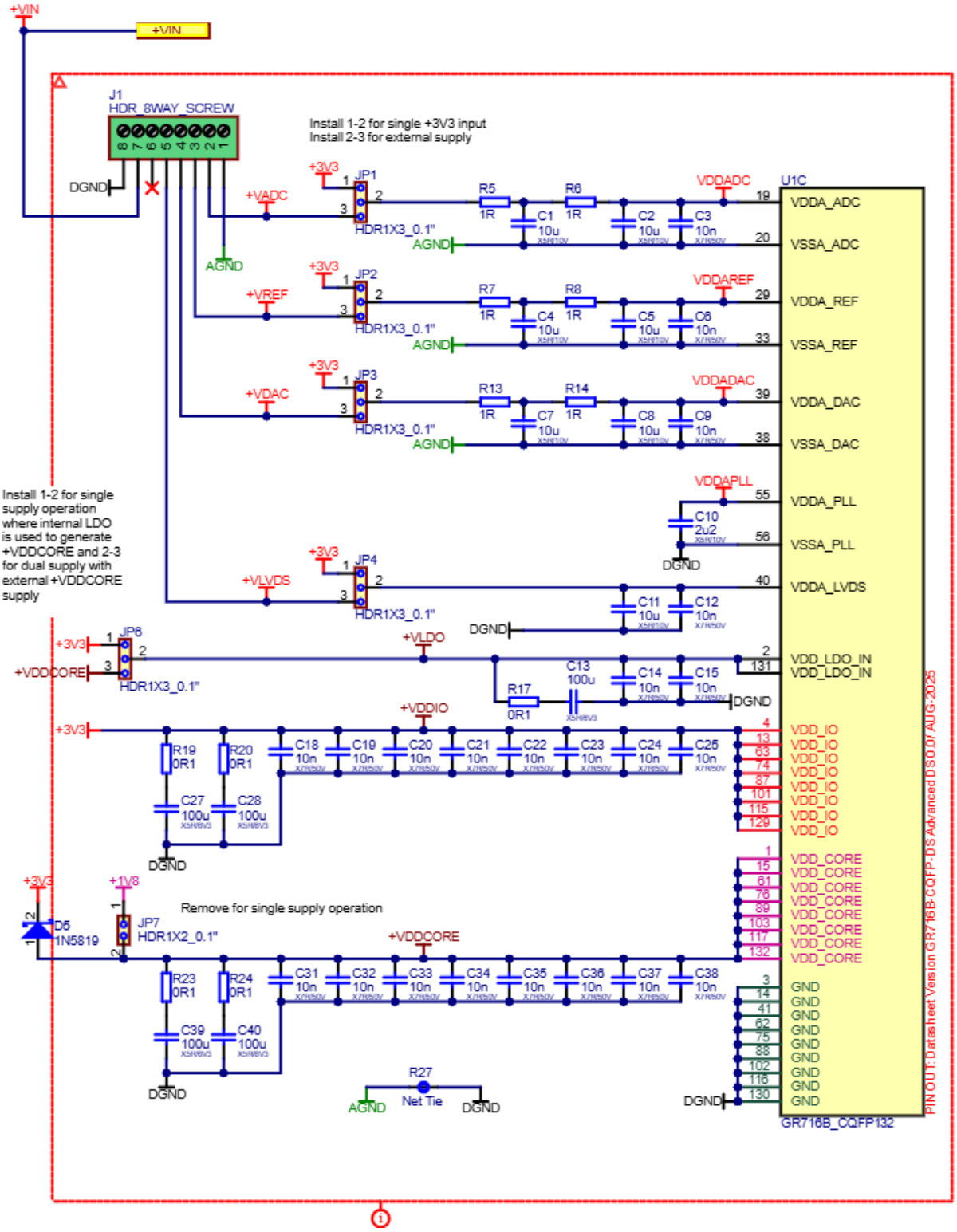

Figure 4-12 Power Supply Configuration Jumpers

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4.11 Reset Circuit and Button

The GR716B microcontroller includes an internal RESET circuit with Brown-out detector to reset the processor and its peripherals (see section 8 of [RD1]).

The resulting low reset signal is present on the microcontroller pin RESET_OUT_N. This signal is connected to the expansion connector, P2.

A manual reset of the microcontroller can be generated using the RESET_IN_N signal. This signal is present on the expansion connector P2 and can be driven from an external circuity if required. A miniature push button switch is provided on the GR716B-DSU-USB (Figure 4-9) to pull this signal low, when the button is pressed.

4.12 Watchdog

The GR716B microcontroller includes an internal Watchdog timer function which can be used for the purpose of generating a system reset in the event of a software malfunction or crash. Please refer to [RD1].

5 SETTING UP AND USING THE BOARD

The board is provided with a default configuration set by bootstrap settings.

For additional information, refer to [RD2] and for information about the Bootstrap signals, refer to section 4.7.

To operate the board, stand alone on the bench top, install the power configuration jumpers appropriately, and +12V supply to the board connector J2.

ATTENTION! To prevent damage to board, please ensure that the correct power supply voltage and polarity is used with the board.

Do not exceed +14.5V at the power supply input, as this may damage the board.

The POWER_3V3 and POWER_1V8 power good LEDs should be illuminated indicating that the power supply is present and the board is generating the supply voltages that it requires.

Upon power on, using default bootstrap the processor will start executing instructions beginning at the memory location 0x02000000, which is the start of the PROM. If the PROM is 'empty' or no valid program is installed, the first executed instruction will be invalid, and the processor will halt with an ERROR condition.

To perform program, download and software debugging on the hardware it is necessary to use the Frontgrade Gaisler GRMON4 debugging software, installed on a host PC (as represented in Figure 4-8). Please refer to the GRMON4 documentation for the installation of the software on the host PC (Linux or Windows), and for the installation of the associated hardware dongle.

To perform software download and debugging on the processor, a link from the Host computer to the DSU interface of the board is necessary. As described in section 4.8 this is achieved via the FTDI USB interface.

Program download and debugging can be performed in the usual manner with GRMON4. More information on the usage, commands and debugging features of GRMON4, is given in the GRMON4 Users Manuals and associated documentation, [RD4].

6 INTERFACES AND CONFIGURATION

6.1 List of connectors

Table 2: List of Connectors

Name	Function	Type	Description
J1	POWER	HDR_8_SCREW	Screw terminals for individual external power
J2	POWER_5V	2.1mm centre +ve	DC power input connector
PI	EXPANSION-1	2x32 pin 0.1” Header	Expansion connector-1
P2	EXPANSION-2	2x32 pin 0.1” Header	Expansion connector-2

Table 3: J1 Screw Terminal Connector for Input Voltages

Pin	Name	Comment
1	AGND	Analog Ground
2	+VADC	+3V3
3	+VREF	+3V3
4	+VDAC	+3V3
5	+VLVDS	+3V3
6	-	Do not apply voltage here
7	+VIN	+5V to +12V
8	**DGND**	Digital Ground

Table 4: J2 POWER-External Power Connector

Pin	Name	Comment
+VE	+VIN	Inner Pin, +5V to +12V, typically 1 A
-VE	**DGND**	Outer Pin Return

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Table 5: Expansion connector P1 Pin-out

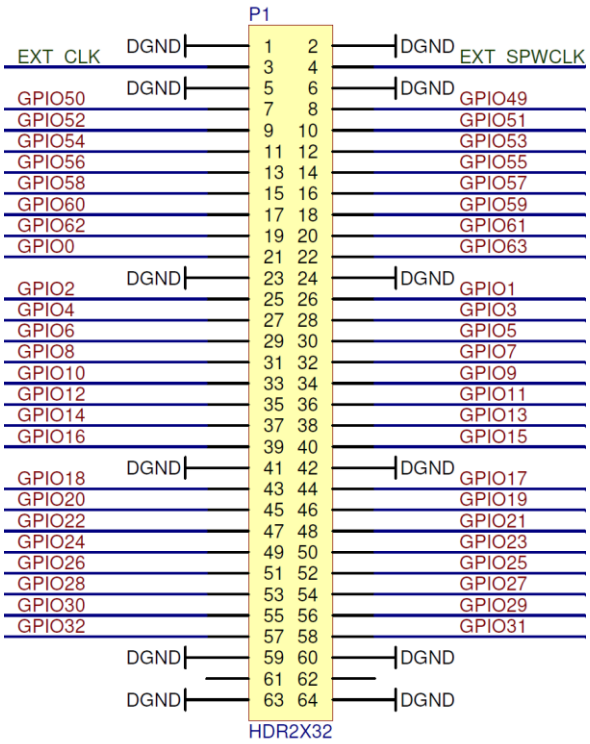
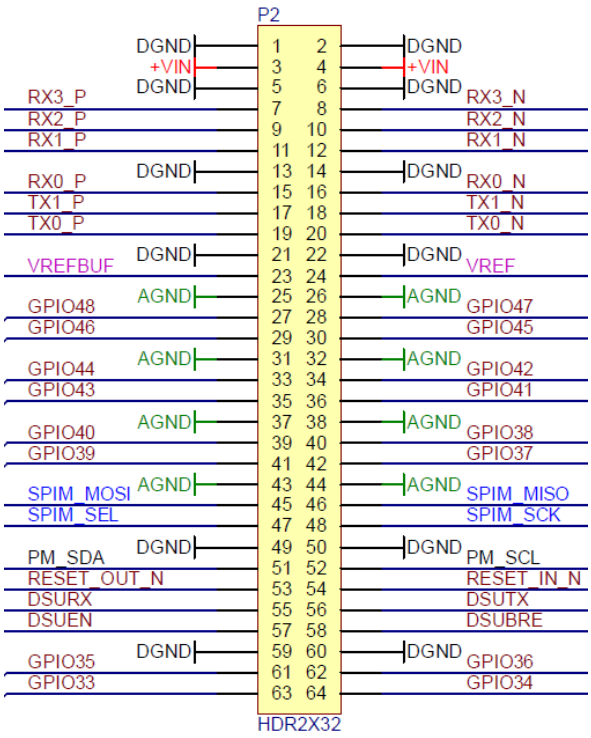


Table 6: Expansion connector P2 pin-out



6.2 List of Oscillators, Switches and LED's

Table 7: List and definition of Oscillators and Crystals

Name	Function	Description
Y1	XTAL	8 pin DIL socket for 5-25 MHz crystal

Table 8: List and definition of PCB mounted LED's

Name	Function	Description
D1	RESET_OUT	Processor RESET_OUT signal
D2	POWER_3V3	3.3V power good
D3	POWER_1V8	1.8V power good

Table 9: List and definition of Switches

Name	Function	Description
S1	8 pole SPST DIP switch	Pull-up/Pull-Down Bootstrap settings – see 4.7
S2	4 pole SPST DIP switch	Pull-up/Pull-Down Bootstrap settings – see 4.7

Table 10: Definition of Switch S1 and S2 switch for bootstrap functions (refer to [RD1])

Switch	Pin	Function	Default
S1-1	GPIO0	Disable EDAC	Up
S1-2	GPIO1	CAN-FD bus Primary or Redundant	Down
S1-3	GPIO15	CAN-FD/I2C node ID [2]	Down
S1-4	GPIO17	Bypass internal Boot PROM	Down
S1-5	GPIO18	CAN-FD remote boot	Down
S1-6	GPIO62	CAN-FD/I2C node ID [1]	Down
S1-7	GPIO63	Redundant Memory Available	Down
S1-8	DSUTX	Copy ASW image/SPW default frequency	Down
S2-1	SPIM-SEL	Boot Source 0	Down
S2-2	SPIM_SCK	Boot Source 1	Down
S2-3	SPIM_MOSI	Remote Access/Boot from Memory	Down
S2-4	-	Reserved, not used	-

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Table 11: Jumper configuration (refer to [RD1])

ITEM	Default	Description of the default configuration
JP1	1-2	Select power supply for ADC. Refer section 4.10
JP2	1-2	Select power supply for REF. Refer section 4.10
JP3	1-2	Select power supply for DAC. Refer section 4.10
JP4	1-2	Select power supply for LVDS. Refer section 4.10
JP5	NC	Not available
JP6	1-2	Select power supply for LDO. Refer section 4.10
JP7	NC	Select power supply for VDDCORE. **Remove for single supply operation.** Refer section 4.10
JP8	NC	Select internal reference (VREFBUF) Always leave JP8 open when connecting GR716B-BOARD with the GR716B-DEV board.
JP9	NC	External Reference sense (VREF)
JP10	1-2	Select system clock source (CLK)
JP11	1-2	Select PLL clock source (SPWCLK)
JP12	NC	Write protect SPI PROM
JP13	1-2	Install to provide onboard power to 3V3

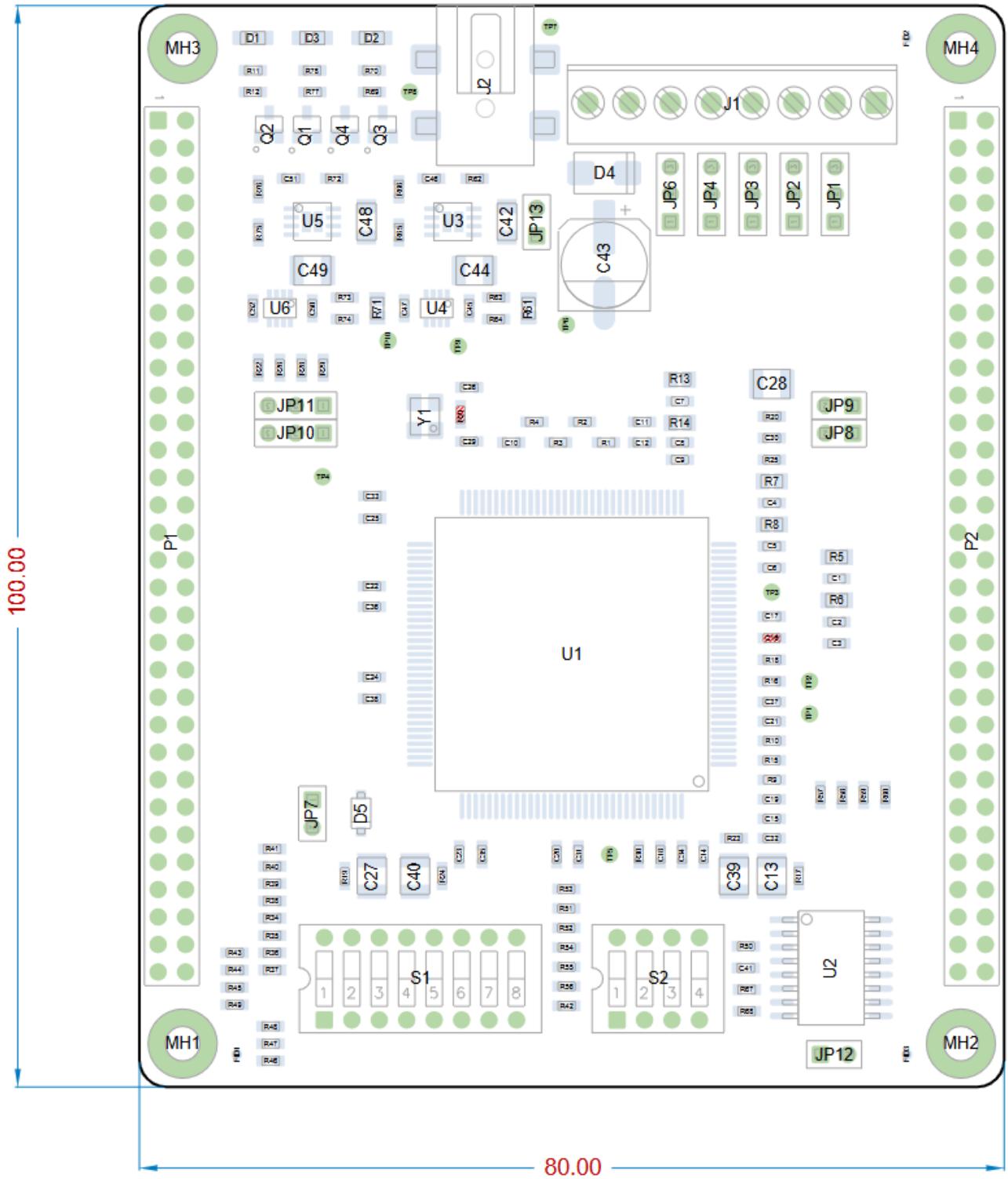

Figure 6-1 PCB Top View

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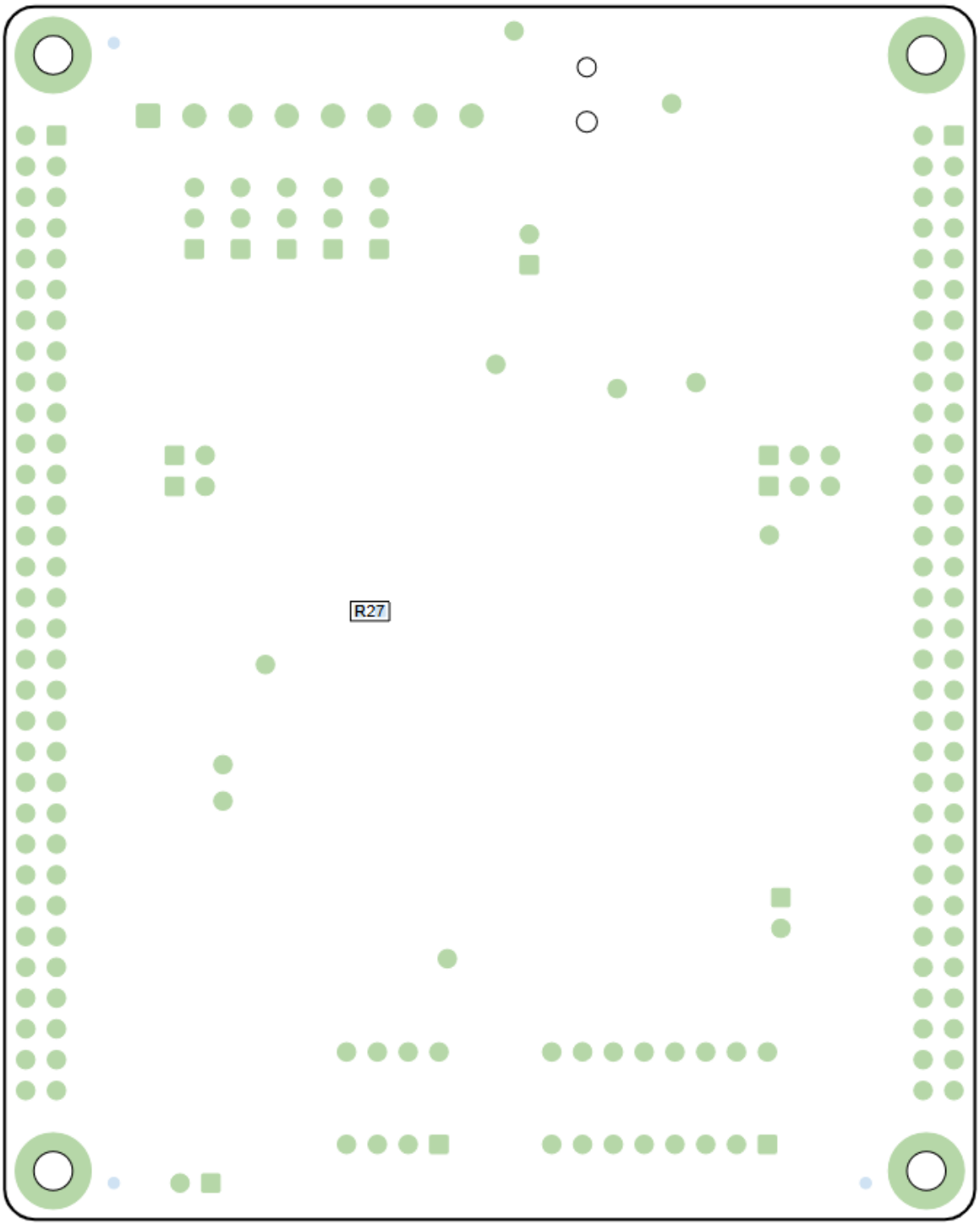

Figure 6-2 PCB Bottom View

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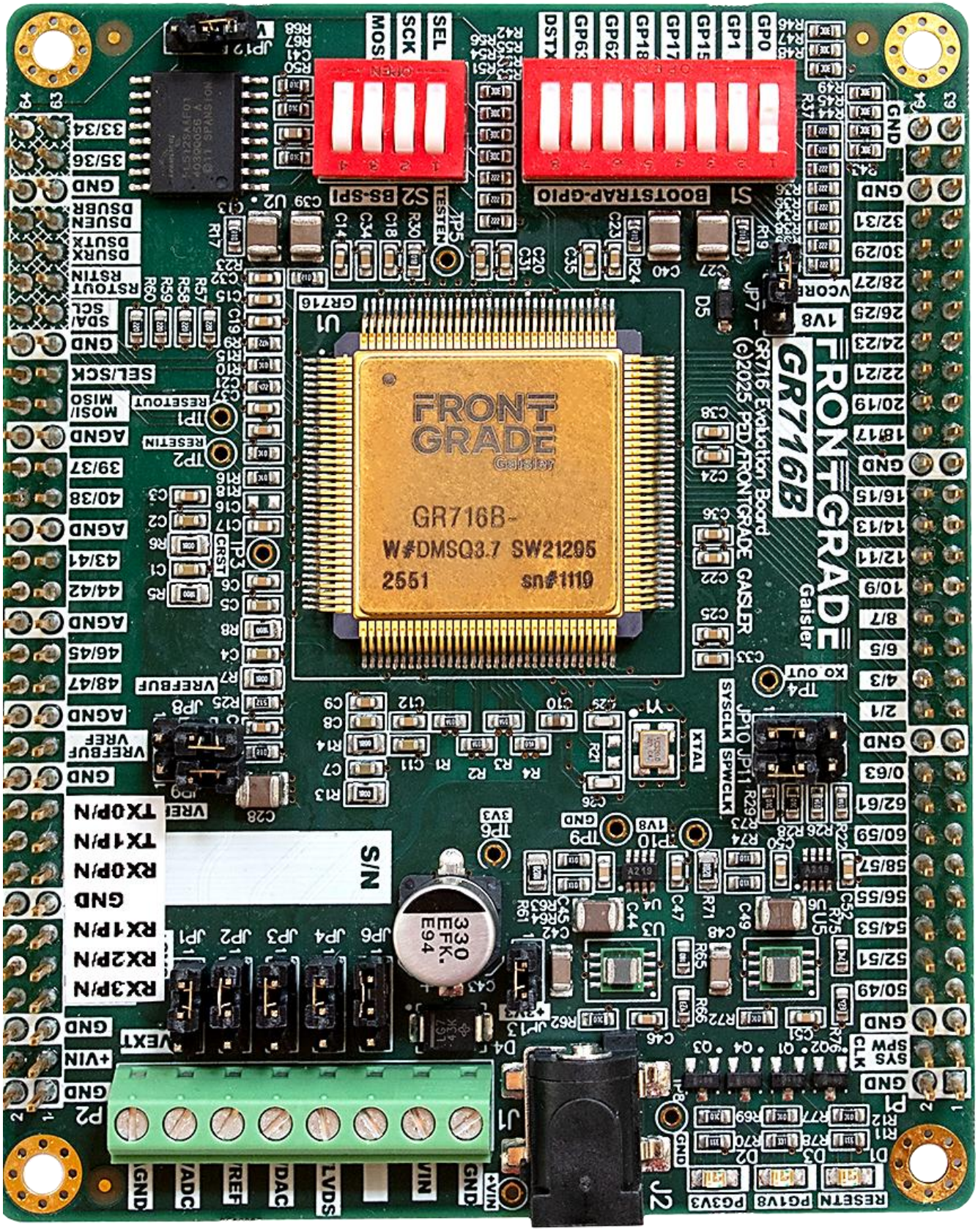

Figure 6-3 GR716B-BOARD Top View (Photo)

Figure 6-4 GR716B-BOARD Bottom View (Photo)

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REVISION INFORMATION

Issue	Date	Section / Page	Description
0.1	June 2024	All	Draft Issue
1.0	2025-12-09		First approved issue
1.1	2026-05-29	Several sections	Board with PCB Revision 2.0 Added information about the boot strap signals (extra switches needed for GR716B) Jumper configuration modifications explained J1 Input Voltages modifications explained The crystal on board is fixed to be 20 MHz

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