GR716B-MIDI Board User's Manual

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USER'S MANUAL

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1 INTRODUCTION

1.1 Purpose and Scope of the Document

This document provides a User's Manual and interface document for the *GR716B-MIDI* development board.

The work has been performed at Frontgrade Gaisler AB, Gothenburg, Sweden.

1.2 Reference Documents

The following documents are referred as they contain relevant information:

[RD1] "GR716B user manual", available from https://www.gaisler.com/products/gr716b

[RD2] GRMON4 User Manual, available from https://www.gaisler.com/products/grmon4

[RD3] "CertusPro-NX Family, Data Sheet", Document number: FPGA-DS-02086 available from https://www.latticesemi.com

[RD4] "sysCONFIG User Guide for Nexus Platform, Technical Note", Document number: FPGA-TN-02099-2.5, available from https://www.latticesemi.com/

[RD5] "CertusPro-NX High-Speed I/O Interface, Technical Note", Document number: FPGA-TN-02244-1.1, available from https://www.latticesemi.com/

2 ABBREVIATIONS

AHB	Advanced High-performance bus, part of [AMBA]
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus, part of [AMBA]
DDR3	Double Data Rate
DSU	Debug Support Unit
EDAC	Error Detection and Correction
ESD	Electro-Static Discharge
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Logic Array
FTDI	Future Technology Devices International
GMII	Gigibit Media Independent Interface
GPIO	General Purpose Input / Output
HCSL	High speed Current Steering Logic
HPC	High Pin Count
I^2C	Inter-Integrated Circuit
IP	Intellectual Property
JTAG	Joint Test Action Group
LPC	Low Pin Count
LVDS	Low-Voltage Differential Signaling
MII	Media Independent Interface
SDRAM	Random Access Memory
SPI	Serial Peripheral Interface
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PHY	Physical Layer Device
PLL	Phase Locked Loop
PROM	Programmable Read Only Memory
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus

3 GR716B-MIDI board design

3.1 Overview

This document describes the design and implementation of the *GR716B-MIDI* board.

The *GR716B-MIDI* board is a compact evaluation platform built around the Frontgrade GR716B radiation-hardened microcontroller featuring the fault-tolerant LEON3 SPARC V8 processor and Lattice Semiconductor FPGA CertusPro-NX. The board is designed with multiple electrical functions and interfaces which gives the user a flexibility to interact with the board.

The board contains the following main items.

- USB-C connectors for debug and power
- GR716B Microcontroller
  - 1 x USB interface via *FTDI FT4232* providing UART
  - 1 x Ethernet for communication[1]
  - 1 x SpaceWire to FMC+ connector
  - 1 x On-board Thermistor
  - 2 x On-board LEDs
  - 3 x On-board MMCX connector (2 x ADC, 1 x DAC)[1]
  - 43 x GPIO to FMC+ connector[1]
  - 64Mb MRAM
  - 512Mb SPI FLASH
- CertusPro-NX FPGA
  - 1 x USB interface via *FTDI FT4232* providing JTAG and UART
  - 1 x Ethernet for communication and debug
  - 4 x On-board MMCX connector (4 x ADC)
  - 4 x SerDes to FMC+ connector
  - LVDS to FMC+ connector
  - 3V3 IO to FMC+ connector
  - I^2C link to FMC+ connector
  - 1GB DDR3 memory
  - 512Mb SPI FLASH
  - 4 x On-board LED
- Intercommunication between GR716B and CertusPro-NX
  - 1 x SpaceWire
  - SPI (to configuration area on FPGA)[2]
  - 5 x GPIO[2]

[1] GR716B has interface that shares pins, refer to section *4.7.3 Pin multiplexing*

[2] It is an onboard multiplexer setting the interface to the FPGA, refer to section *4.8.1 Configurate and programming*

3.2 Handling

ATTENTION: OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES

This unit contains sensitive electronic components which can be damaged by Electrostatic Discharges (ESD). When handling or installing the unit observe appropriate precautions and ESD safe practices.

When not in use, store the unit in an electrostatic protective container or bag.

When configuring the jumpers on the board, or connecting/disconnecting cables, ensure that the unit is in an un-powered state.

When operating the board in a 'stand-alone' configuration, the power supply should be current limited to prevent damage to the board or power supply in the event of an overcurrent situation.

This equipment has SpaceWire ports that use Low Voltage Differential Signalling (LVDS) which has limited common mode voltage protection. To avoid damage to the SpaceWire interfaces due to common mode voltage see section 4.9 FMC+ connector

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4 BOARD DESIGN

This section describes the board design in detail. The electrical functions and interfaces that are common for both the devices (the Microcontroller and the FPGA) are described in the first sections: 4.1 to 4.6. In section 4.7 and 4.8 each device and corresponding functions/interfaces are described. The FMC+ connector is described in section 4.9.

Note: This design is not aimed for flight and should not be used as a reference design.

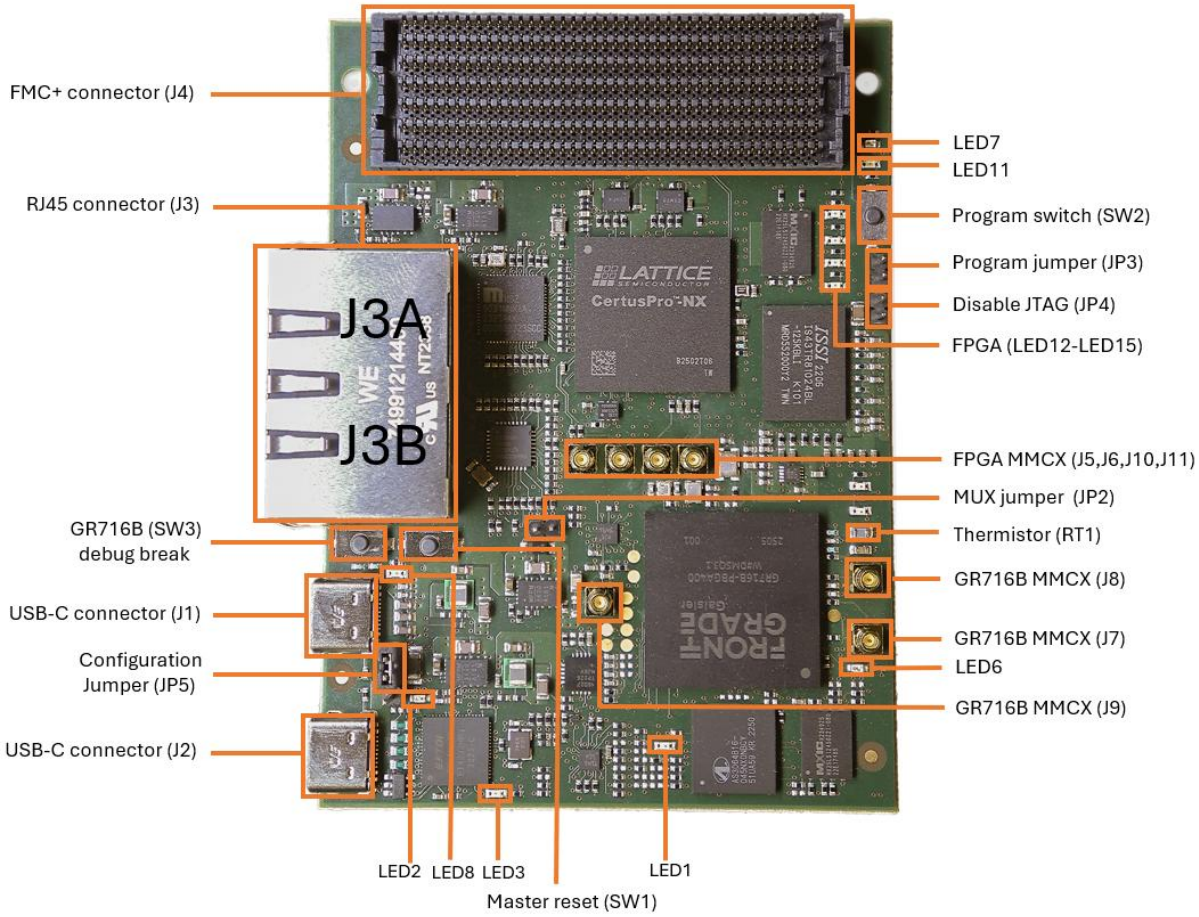

Figure 4-1 Top view of GR716B-MIDI board

Figure 4-1 shows the top view for the *GR716B-MIDI* board and is marked with interactions and indications. For a more detailed assembly drawing referring to Appendix A & B.

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4.1 Board block diagram

The *GR716B-MIDI* Development Board provides the electrical functions and interfaces as represented in the block diagram in Figure 4-2.

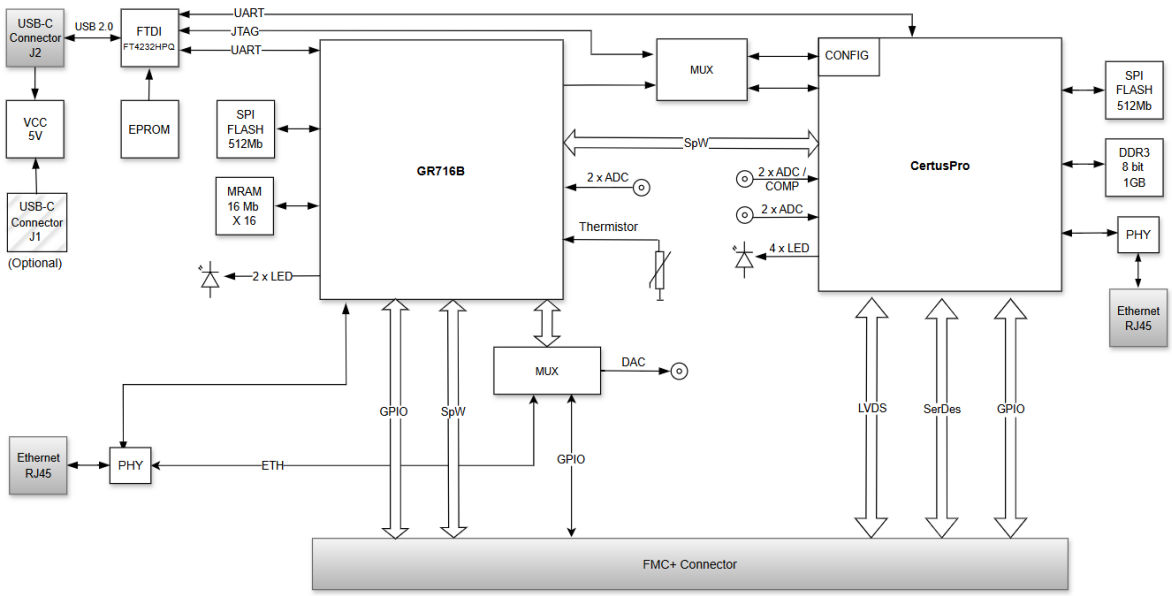

Figure 4-2 GR716B-MINI Board block Diagram

There are multiple ways to communicate with the board, in Figure 4-2 the connectors are represented as grey boxes and described shortly below.

1. **USB 2.0**: The USB 2.0 link is connected to a FTDI chip that converts the USB-data into three serial outputs (1 x JTAG and 2 x UART) connected to both the FPGA and Processor. USB 2.0 interface is connected to connector J2.

2. **Ethernet**: The board is equipment with two RJ45 connectors where J3B connects to the GR716B that supports MII and J3A to the FPGA that support MII and GMII.

3. **FMC+ connector**: the usage of the FMC+ connector is dependent on an external mezzanine board. In this design the FMC+ connector provides the GR716 with one SpaceWire channel and GPIO signals, the CertusPro-NX with SerDes, LVDS, I^2C and GPIO 3V3.

4.2 Power the board

The GR716B-MIDI board is powered using either of the USB-C connectors (J1 or J2). Therefor there are two ways to power supply the board, and which is accomplished by attaching a 2-pin jumper to the 3-pin head (JP5), see Figure 4-3

The overall power requirement for the board is 15W. J2 is considered as the main power supply, and the configuration jumper is set to this as default (JP5: 1-2). This can be used when communicating with USB-C (data and power through the same cable), Ethernet or FMC+ connector. The USB-C source must handle at least 3A, 5V (15W). J2 must be inserted to start up the board since the D_N/P signals are needed to the FTDI chip see Figure 4-3.

There is only one exception when there is need to use J1 as power source. This is when the user is communicating with USB and the USB-source (for example a computer or a docking station) cannot handle the power requirements. Then, the users need to have an external power source connected to J1 and the data to J2, this configuration is chosen when setting jumper in JP5: 2-3 mode.

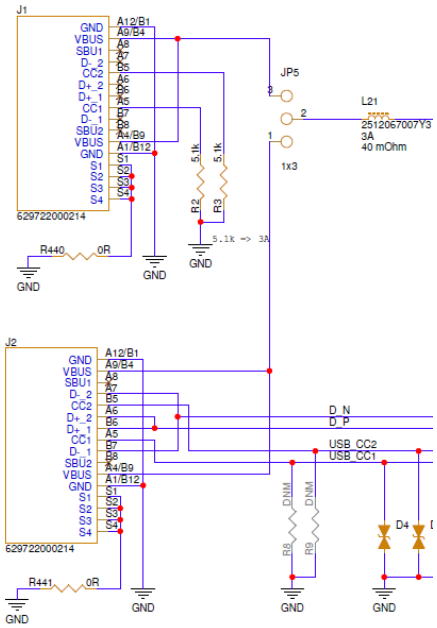

Figure 4-3 USB-C connector for power supply solution

Note: that the source (for example a computer, charger or docking station) used in this case must have a USB-C connector that can deliver **at least 3A, 5V (15W)**. Observe that not all sources with USB-C sockets support that. Check the sources manual before connecting to the *GR716B-MIDI* board.

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4.3 Interacting with the board

As mentioned in section 4.2 there are two ways to power supply the board, by setting a configuration jumper. This configuration jumper is shown in Figure 4-4.

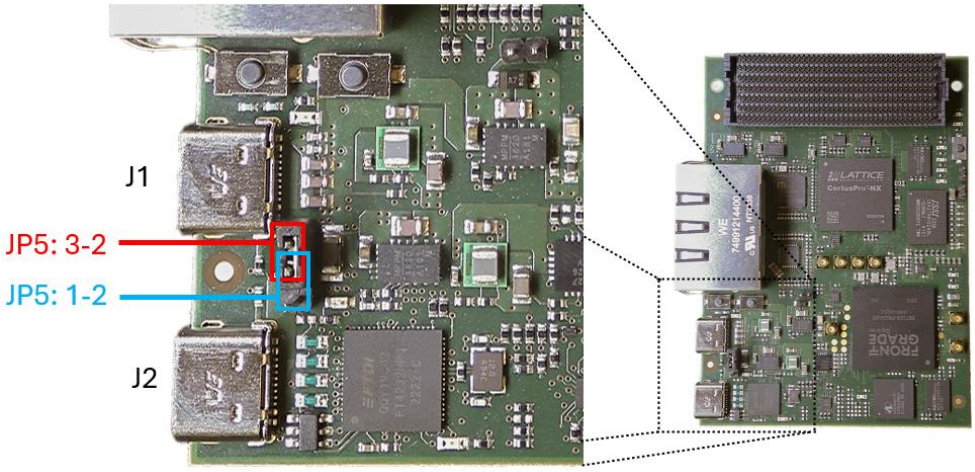

Figure 4-4 Jumper Configuration

On the board there are four LED for indicating power availability and USB communication status, see Table 4-1 for more information and Figure 4-5 for the component's placement.

Table 4-1 Power and status LED

LED	Colour	Description
LED1	Green	Indicates that 3V3 is available
LED2	Red	Light when USB is in suspended mode
LED3	Green	Indicate normal operational mode.
LED8	Green	Indicates that 5V is available

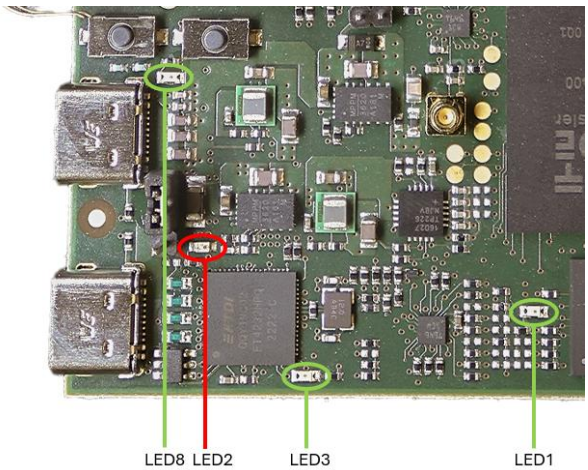

Figure 4-5 Power and USB - LED board placement

4.4 Power supplies

A block diagram showing the power supply design for the *GR716B-MIDI* board is shown in Figure 4-6. Since this board is power supplied through USB the FTDI chip that handles the communication via USB is powered up first via a dedicated voltage. A GPIO from the FTDI chip goes HIGH after the handshake is performed with OK result. This signal enables the rest of the power supplies through a voltage sequencer. The voltage sequencer (MAX16027TP+) will enable the different voltages in specific order with a fixed time delay set by an external capacitor. The GR716B component can be either power supplied in dual or single mode. As default the component is supplied in dual mode, meaning that both 1.8V and 3.3V are applied. The board can by change resistors also be configured to supply the GR716B in single mode. In single mode the GR716B component is supplied from 3.3V only and the 1.8V is created by an internal LDO.

To achieve the right power setup to the DDR3 memory interface a dedicated DDR3 termination circuit (TPS51200) is used.

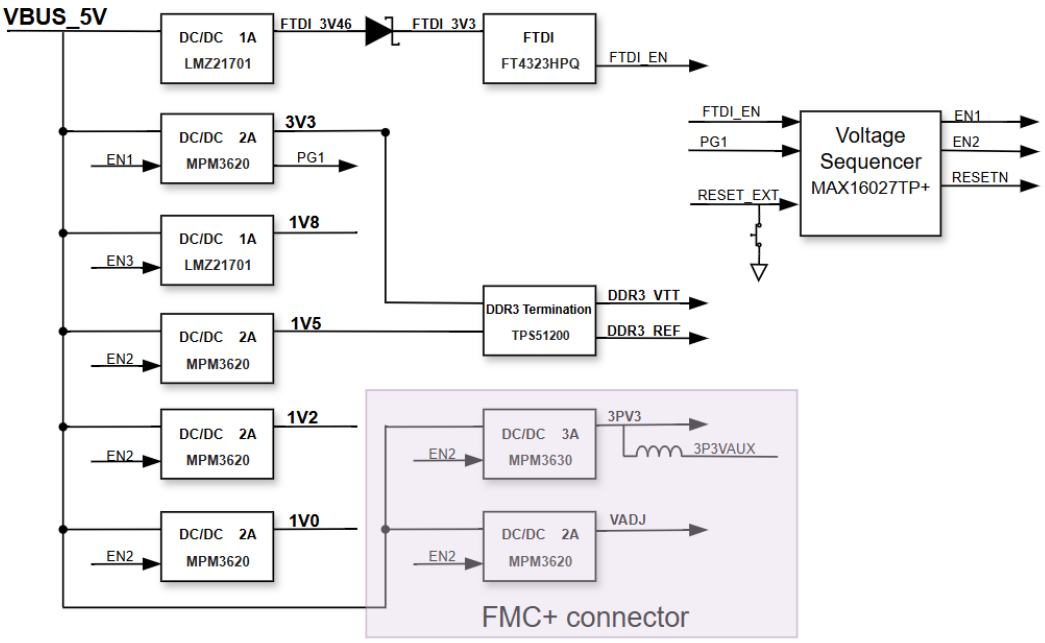

Figure 4-6 Power Regulation Scheme

Table 4-2 below list the different voltages for the GR716B-MIDI board with their main users.

Table 4-2 Voltages

Voltage	Main users
FTDI_3V46	FTDI chip, EPROM
FTDI_3V3	FTDI chip
3V3	Oscillators, Micro Processor (GR716B), MUX, MRAM, Ethernet PHY, SPI FLASH, FPGA (CertusPro-NX), DDR3 termination regulator
3PV3	FMC+ Connector
3PV3AUX	FMC+ Connector
1V8	Micro Processor (GR716B), FPGA (CertusPro-NX)
1V5	FPGA (CertusPro-NX), DDR3 Termination, DDR3 Memory
1V2	Ethernet PHY
1V0	FPGA (CertusPro-NX)
VADJ (1.8V)	FMC+ Connector, FPGA (CertusPro-NX)

4.5 FTDI chip

The *GR716B-MIDI* board provides Serial to USB interface chip, FT4232HPQ from FTDI, which provides multiple serial ports connect to a single USB-C connector (J2). The FTDI chip is connected to the GR716B with UART and to the CertusPro-NX with both JTAG and UART. There are three signals connected to the FTDI chip in addition to the interfaces, see Table 4-3 for the port and signal assignments. There is an EEPROM connected to the FTDI chip aimed for configuration. A separate 12 MHz crystal is dedicated for the FTDI chip.

Table 4-3 FTDI Port assignment

Port	Pin name	Signal name	Target
A	ADBUS6 ADBUS7	RESET DSUBREAK	RESET sequencer GR16B
B	BDBUS0 BDBUS1 BDBUS2 BDBUS3 BDBUS7	JTAG_1.TCK JTAG_1.TDI JTAG_1.TDO JTAG_1.TMS PROGRAMN	CertusPro-NX CertusPro-NX
C	CDBUS0 CDBUS1	UART_0.RXD UART_0.TXD	GR716B
D	DDBUS0 DDBUS1	UART_1.RXD UART_1.TXD	CertusPro-NX

The corresponing "vendor id" is 0403 and "product id" is 6043 for the FTDI chip. Verify that the board is recognized by the host computer. In windows go to Device Manager, in linux use the lsusb command in the terminal

Please see GRMON4 User's Manual for how to set up the required FTDI driver software and how to connect with the device.

4.5.1 Common Mistakes / Know issues

Why is there no /dev/ttyUSB on Linux?
On Linux, the ftdi_sio kernel module is responsible for creating /dev/ttyUSB. Prior to kernel version 6.1 ftdi_sio does not automatically recognize the FT4232HP serial converter that is used on the GR716B-MIDI board. However, in earlier versions of Linux it is possible to temporarily (persisting until reboot) add support for the FT4232HP by adding the corresponding USB VID:PID identification to the driver. This can be done with the below command:

>>> echo 0403 6043 > /sys/bus/usb-serial/drivers/ftdi_sio/new_id

"invalid cable"
On Linux this happens when the USB device is in use by another program. This can for example happen if another instance of GRMON is already connected to the selected cable. But the more common situation is that the ftdi_sio kernel module has attached it to a /dev/ttyUSB serial device. The availability for all ports can be printed with the command "grmon -ftdi -jtaglist". Whether the ftdi_sio module is attached to a particular port can be seen in the output of "lsusb -t". The ftdi_sio module can unloaded using

>>> rmmod ftdi_sio

which will detach all /dev/ttyUSB serial ports and make them available for use by GRMON. It is also possible to selectively detach the /dev/ttyUSB corresponding to the desired port using the shell-script "ftdi_sio_detach.sh". This script can be found in the share-folder in the GRMON installation. Typically "grmon-pro-4.x.x/linux/share/ grmon/tools/ftdi_sio_detach.sh". To remove /dev/ttyUSB0:

>>> ./ftdi_sio_detach.sh /dev/ttyUSB0

4.6 Reset

The reset signal is active low and is connected to the GR716B, CertusPro-NX, both ethernet PHY and it is derived from the voltage sequencer. The reset signal is held low by the sequencer until all the enable (output) signals are high. The reset signal is controlled by a master-reset (input) signal. This signal is also active low and have a pull-up resistor connected to it. There is a switch (SW1) for manually reset the board and an external signal from the FTDI chip for remote reset connected to the master-reset. The remote signal is connected to pin ADBUS6 on the FTDI chip, feature allows GRMON to use the flag -ftdigpio

4.7 GR716B Micro Processor

The GR716B is a radiation-hardened microcontroller featuring the fault-tolerant LEON3 SPARC V8 processor.

For more information about the GR716B such as interfaces, operation and programming see the Data sheet [RD1].

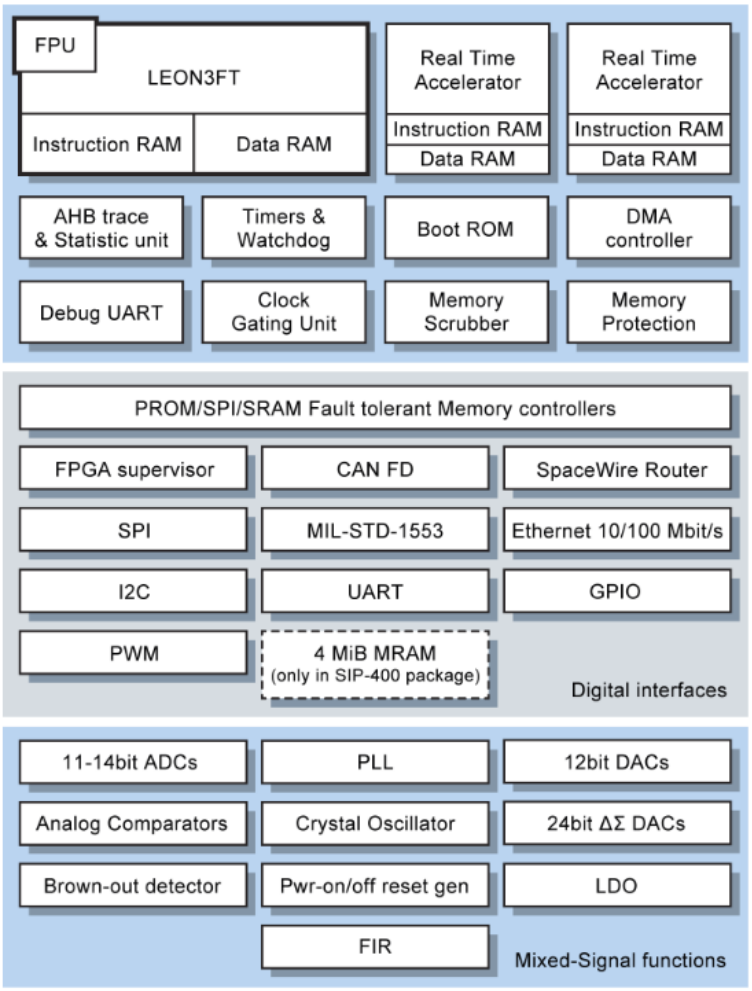

Figure 4-7 GR716B block diagram

The GR716B is available in different packages, on the GR716B-MIDI board the BGA package is implemented. With the BGA version of the component more signals have dedicated pins, for example the memory interface and LVDS.

4.7.1 Bootstrap signals

The power-up and initialisation state for the GR716B is affected by several external signals. Several GPIO and function pins are predefined for this purpose. For more detailed information about the bootstrap signals see section 3.1 in GR716B User Manual [RD1]. On the board there are options to change all the bootstrap values since there are additional not mounted resistors in the schematic, see Figure 4-8.

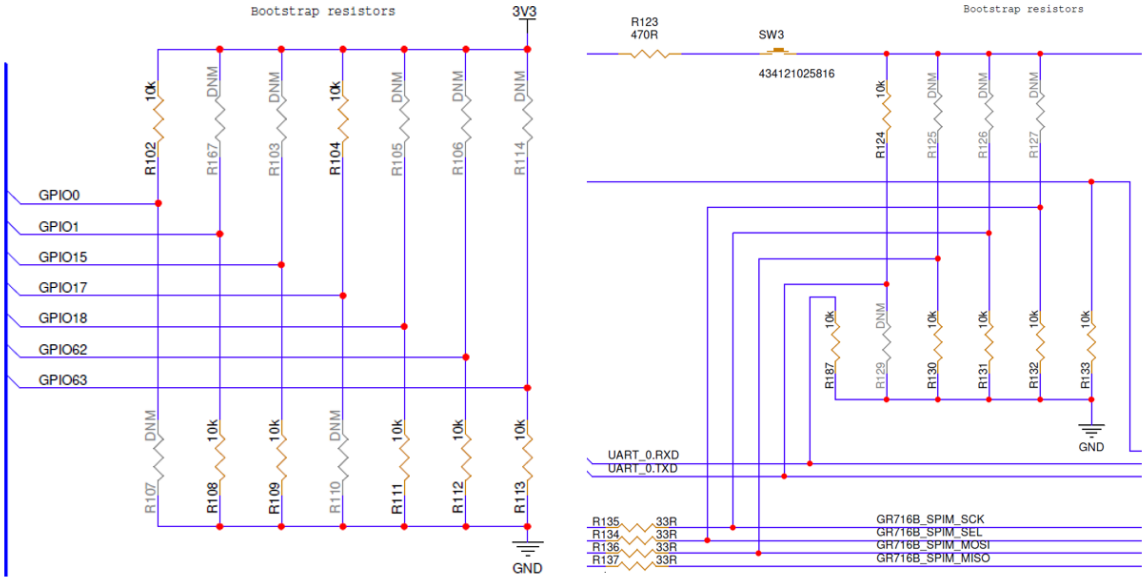

Figure 4-8 Bootstrap for GR716B

The default configuration for those signals in the GR716B-MIDI design is shown in Table 4-4.

Table 4-4 Default bootstrap values

Bootstrap signal	Default	Description
DSU_EN	HIGH	Enables the Debug Support Unit (DSU)
DSU_BREAK	LOW	Puts all processors in debug mode when asserted
GPIO[0]	HIGH	EDAC for external boot RAM disabled. Determines the use of EDAC for external boot RAM when Bit 0 of the CAN-FD and I2C node ID (ID[2]).
GPIO[1]	LOW	Nominal bus for CAN-FD
GPIO[15]	LOW	Bit 2 of the CAN-FD and I2C node ID (ID[2]).
GPIO[17]	HIGH	Enable bypass of internal boot ROM. Booting from external SPI memory
GPIO[18]	LOW	CAN-FD remote boot disabled.
GPIO[62]	LOW	Test of internal memories at startup disabled. Bit 1 of the CAN-FD and I2C node ID (ID[2]).
GPIO[63]	LOW	Extra protection of external boot source disabled.
DUART_TXD	HIGH	Copy ASW image from selected external boot memory.
SPIM_MOSI	LOW	Remote access is disabled.
SPIM_SCK & SPIM_SEL	LOW	Boot from external SPI memory selected

4.7.2 Debugging

The debug interface provided for the GR716B is UART. On the GR716B-MIDI board this can be accessible via USB through the FTDI chip, refer to section *4.5 FTDI chip*

Program download and debugging to the processor is performed using the GRMON4 Debug Monitor tool from Frontgrade Gaisler [RD2]. For more information about the debugging referring to the GRMON4 documentation [RD2]

There are two debug control signals to the GR716B

1. DSU_EN (input): This signal is a bootstrap signal which is pulled high on the board to enable debugging.

2. DSU_BREAK (input): This signal puts all processors in debug mode when asserted while DSU_EN is HIGH. On this board the signal is pull-down, it can manually be asserted by a switch (SW3). This signal is also connected to pin ADBUS7 on the FTDI chip, this feature allows GRMON to break the reset-loop by the flag -ftdigpio

4.7.3 Pin multiplexing

Due to a limited numbers of pins in the GR716B package, some interfaces share pins. This leads to certain limitations in which interfaces can be used simultaneously. Since the GR716B-MIDI board have some fix interfaces/functionalities on the board there are some signals that will not be able to access on the board. Table 4-5 list the fully compatibility for the multiplexing between the GR716B component and the GR716B-MIDI board. Where the signals that are not accessible have a crossover and coloured in grey. Note, some signals have multiple functions or are multiplexed on board

Since this is the BGA package of GR716B the MUX-option for the memory interface is excluded in Table 4-5 since theses have dedicated pins. There are also two external multiplexer on the board to be able to switch between interfaces show in Figure 4-2, more details about the two multiplexers can be found in section *4.7.12 Ethernet* and *4.8.1 Configurate and programming*

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Table 4-5 GR716B-MIDI board compatibility with GR716B interface

BOARD Functions						GR716B Pin-mux available													
FMC+	Boot-strap	ETH	FPGA	ADC/ DAC	LED	0x0	0x1	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xA	0xB	0xC	0xD	0xE	0xF
✓	✓					GPIO0	UART_RTSN0	1553_RXENA	PWRX_BUSYN	CAN_TX0		SPIM_SLV1			SYNC_1	ALARM_0	tACOMP_FAST			
✓	✓					GPIO1	UART_CTNS0	1553_TXA	PWRX_CLK	CAN_RX0		SPIM_SCK1		AB0_A	CF0_C	G_0				
✓						GPIO2	UART_TX0	1553_RXA	PWRX_DATA	CAN_SEL0	I2CM_SDA0	SPIM_MOSI1		AB0_B	CF0_D	G_1	tDAC_I_D0			
✓						GPIO3	UART_RX0	1553_RXNA	PWRX_ABORT	CAN_RX1	I2CM_SCL0	SPIM_MISO1		AB1_A	CF0_E	G_2	tDAC_I_D1			
✓						GPIO4	UART_CTSN1	1553_TXNA	PWRX_VALID	CAN_TX1	I2CM_SDA1	SPI_SCK0		AB1_B	CF0_F	G_3	tDAC_I_D2			
✓						GPIO	UART_RTSN1	1553_TXINHA	PWRX_RDY	CAN_SEL1	I2CM_SCL1	SPI_MISO0		A0_0	CF1_C	G*_0	tDAC_I_D3			
✓						GPIO6	UART_TX1	1553_RXB	PWTX_VALID		I2CS_SDA0	SPI_MOSI0		A0_1	CF1_D	G*_1	tDAC_I_D4			
✓						GPIO7	UART_RX1	1553_RXNB	PWTX_CLK		I2CS_SCL0	SPI_SEL0		A0_2	CF1_E	G*_2	tDAC_I_D5			
✓						GPIO8	UART_CTSN2	1553_RXENB	PWTX_BUSYN		I2CS_SDA1	SPI_SLV0_0		A0_3	CF1_F	G*_3	tDAC_I_D6			
✓						GPIO9	UART_RTSN2	1553_TXB	PWTX_READY		I2CS_SCL1	SPI_SLV0_1		DAC0_CLK	CF2_C	G*_4	tDAC_I_D7			
✓						GPIO10	UART_TX2	1553_CLK	PWTX_DATA		I2CS_SDA2	SPI_SLV0_2		DAC0_A	CF2_D	G*_5	tDAC_I_D8			
✓						GPIO11	UART_RX2	1553_TXNB	PWTX_ABORT		I2CS_SCL2	SPI_SLV0_3		DAC0_B	CF2_E	G*_6	tDAC_I_D9			
✓						GPIO12		1553_TXINHB						DAC0_C	CF2_F	G*_7	tDAC_I_D10			
			✓			GPIO13	UART_CTSN3			CAN_TX0		SPI_SCK1		DAC1_CLK	G_0	G*_8	~~tDAC_I_D011~~			
			✓			GPIO14	UART_RTSN3			CAN_RX0		SPI_MISO1		DAC1_A	G_1	G*_9	~~tADC_O_D0~~			
	✓		✓			GPIO15	UART_TX3			CAN_SEL0		SPI_MOSI1		DAC1_B	G_2	G*_10	~~tADC_O_D1~~			
			✓			GPIO16	UART_RX3			CAN_RX1		SPI_SEL1		DAC1_C	G_3	G*_11	~~tADC_O_D2~~			
	✓		✓			GPIO17	UART_RTSN4			CAN_TX1		SPI_SLV1_0			ALARM_2	SYNC_0	~~tADC_O_D3~~			
✓	✓					GPIO18	UART_TX4			CAN_SEL1		SPI_SLV1_1		AB2_A	G*_0	CF0_C	tADC_O_D4			
✓						GPIO19	UART_RX4							AB2_B	G*_1	CF0_D	tADC_O_D5	TDP_SETET	tPLL_LOCK	
					✓	GPIO20	~~UART_CTSN4~~							~~AB3_A~~	~~G*_2~~	~~CF0_E~~	~~tADC_O_D6~~	~~TDP_E_ET_I~~	~~tSCRUB_CLK~~	
					✓	GPIO21	~~UART_CTSN5~~					~~SPI_SLV1_2~~		~~AB3_B~~	~~G*_3~~	~~CF0_F~~	~~tADC_O_D7~~		~~tMIL_CLK~~	
✓						GPIO22	UART_RTSN5					SPI_SLV1_3		DAC2_CLK	G*_4	CF1_C	tADC_O_D8		tSPW_CLK	
✓						GPIO23	UART_TX5							DAC2_A	G*_5	CF1_D	tADC_O_D9		tSYS_CLK	
✓						GPIO24	UART_RX5							DAC2_B	G*_6	CF1_E	tADC_O_D10			
✓						GPIO25			PWRX_VALID		I2CM_SDA0	SPI_SCK0		DAC2_C	G*_7	CF1_F	tADC_O_EOC		SCRUB_INITN	
✓						GPIO26			PWRX_CLK		I2CM_SCL0	SPI_MISO0		DAC3_CLK	G*_8	CF2_C	tADC_O_CMP		SCRUB_DONE	
✓						GPIO27			PWRX_DATA		I2CM_SDA1	SPI_MOSI0		DAC3_A	G*_9	CF2_D	tBO_O		SCRUB_DATA0	
✓						GPIO28			PWRX_ABORT		I2CM_SCL1	SPI_SEL0		DAC3_B	G*_10	CF2_E	CLKDET_OK		SCRUB_DATA1	
✓						GPIO29			PWRX_BUSYN		I2CS_SDA0	SPI_SLV0_0		DAC3_C	G*_11	CF2_F	CLKDET_RO0		SCRUB_DATA2	RINGOSC0
✓						GPIO30			PWRX_RDY		I2CS_SCL0	SPI_SLV0_1		ALARM_2	SYNC_0	AB0_A	CLKDET_E0		SCRUB_DATA3	
✓						GPIO31			PWTX_VALID		I2CS_SDA1	SPI_SLV0_2		SYNC_1	ALARM_0	AB0_B	CLKDET_RO1		SCRUB_DATA4	RINGOSC1
✓						GPIO32			PWTX_CLK		I2CS_SCL1	SPI_SLV0_3		A0_0	ALARM_1	SYNC_1	CLKDET_E1		SCRUB_DATA5	

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✓						GPIO33	UART_CTSN3		PWTX_BUSYN		I2CM_SDA0			A0_1	DAC0_CLK	AB1_A	LVDS_FSRX		SCRUB_DATA6	
✓						GPIO34	UART_RTSN3		PWTX_READY		I2CM_SCL0			A0_2	DAC0_A	AB1_B			SCRUB_DATA7	
✓						GPIO35	UART_TX3		PWTX_DATA		I2CS_SDA0			A0_3	DAC0_B	MEM_BRDYN			SCRUB_PROG	
✓						GPIO36	UART_RX3		PWTX_ABORT		I2CS_SCL0			ALARM_3	DAC0_C	MEM_BEXCN			SCRUB_RDWR	
✓						GPIO37	UART_RTSN4	1553_RXENA	PWRX_VALID	CAN_TX0		SPI_SLV0_3	ADC				tACOMP_SET0		SCRUB_CSIN	
✓						GPIO38	UART_TX4	1553_TXA	PWRX_CLK	CAN_RX0		SPI_SLV0_2	ADC						SCRUB_SCLK	
				✓		GPIO39	UART_RX4	1553_RXA	PWRX_DATA	CAN_SEL0	I2CS_SDA1	SPI_SLV0_1	ADC							
				✓		GPIO40	UART_CTSN4	1553_RXNA	PWRX_ABORT		I2CS_SCL1	SPI_SLV0_0	ADC							
✓						GPIO41	UART_CTSN5	1553_TXNA	PWRX_BYN	CAN_TX0	I2CM_SDA0	SPI_SCK0	ADC	AB0_LEB						
✓						GPIO42	UART_RTSN5	1553_TXINHA	PWRX_RDY	CAN_RX0	I2CM_SCL0	SPI_MISO0	ADC	AB1_LEB						
✓						GPIO43	UART_TX5	1553_RXB	PWTX_VALID	CAN_SEL0	I2CS_SDA0	SPI_MOSI0	ADC	AB2_LEB						
				✓		GPIO44	UART_RX5	1553_RXNB	PWTX_CLK	CAN_RX1	I2CS_SCL0	SPI_SEL0	ADC	AB3_LEB						
		✓				GPIO45	UART_RX0	1553_RXENB	PWTX_BUSYN	CAN_RX1		SPI_SLV1_1	DAC0							ETH_TXCLK
		✓				GPIO46	UART_TX0	1553_TXB	PWTX_RDY			SPI_SLV1_0	DAC1							ETH_RXCLK
✓		✓				GPIO47	UART_CTSN0	1553_CLK	PWTX_DATA	CAN_TX1	I2CM_SDA1	SPI_SCK1	DAC2							ETH_MDIO
		✓		✓		GPIO48	UART_RTSN0	1553_TXNB	PWTX_ABORT	CAN_SEL1	I2CM_SCL1	SPI_MISO1	DAC3							ETH_MDC
		✓				GPIO49	UART_CTSN0	1553_TXINHB			I2CS_SDA2	SPI_MOSI1				SPIM_SLV1	AHBUART_TX	TDP_SETET		ETH_INT
		✓				GPIO50	UART_TX0				I2CS_SCL2	SPI_SEL1				SPIM_SCK1	AHBUART_RX	TDP_E_ET_1		ETH_RXD3
		✓				GPIO51	UART_RX0	1553_RXENA				SPI_MOSI1	ADC	AB0_TEB		SPIM_MOSI1		TDP_PULSE0		ETH_RXD2
		✓				GPIO52	UART_CTSN1	1553_TXA	PWRX_VALID		I2CM_SDA0	SPI_SEL1	ADC	AB1_TEB		SPIM_MISO1		TDP_PULSE1		ETH_RXD1
		✓				GPIO53	UART_RTSN1	1553_RXA	PWRX_CLK		I2CM_SCL0	SPIS_SCK0	ADC	AB2_TEB		SPI4S_SCK1				ETH_RXD0
		✓				GPIO54	UART_TX1	1553_RXNA	PWRX_DATA		I2CM_SDA1	SPIS_MISO0	ADC	AB3_TEB		SPI4S_MISO1				ETH_RXDV
✓		✓				GPIO55	UART_RX1	1553_TXNA	PWRX_ABORT		I2CM_SCL1	SPIS_MOSI0	ADC		A0_LEB	SPI4S_MOSI1	TIMER32_TICKGEN			ETH_RXER
✓		✓				GPIO56	UART_CTSN2	1553_TXINHA	PWRX_BSYN		I2CS_SDA0	SPIS_SLV0	ADC		A1_LEB	SPI4S_SLV1	tEVENT_TRIG			ETH_COL
✓		✓				GPIO57	UART_RTSN2	1553_RXB	PWRX_RDY		I2CS_SCL0	SPI_SCK0	ADC		A2_LEB		tDNCNT24			ETH_CRS
✓		✓				GPIO58	UART_TXN2	1553_RXNB	PWTX_VALID	CAN_TX0	I2CS_SDA1	SPI_MISO0	ADC		A3_LEB		tDNCNT12			ETH_TXD3
✓		✓				GPIO59	UART_RXN2	1553_RXENB	PWTX_CLK	CAN_RX0	I2CS_SCL1	SPI_MOSI0					tTIMER32	tA-COMP_SET1		ETH_TXD2
✓		✓				GPIO60	UART_CTSN3	1553_TXB	PWTX_BUSYN	CAN_SEL0	I2CS_SDA2	SPI_SEL0					tTIMER27	TDP_PULSE2		ETH_TXD1
✓		✓				GPIO61	UART_RXN3	1553_CLK	PWTX_RDY	CAN_RX1	I2CS_SCL2	SPI_SLV0_0					tTIMEALARM	TDP_PULSE3		ETH_TXD0
	✓	✓				GPIO62	UART_TX3	1553_TXNB	PWTX_DATA	CAN_TX1		SPI_SLV0_1					tPARITYERR	TDP_PULSE4		ETH_TXEN
	✓					GPIO63	UART_RTSN3	1553_TXINHB	PWTX_ABORT	CAN_SEL1		SPI_SLV0_2					tAPWM_OUT	TDP_PULSE5		

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4.7.4 LED

There are LEDs connected to the GR716B on the board, see Table 4-6 for more information and Figure 4-1 for the board placement.

Table 4-6 LED correspond the GR716B

LED	Colour	Description
LED4	Green	Connected to GPIO20
LED5	Green	Connected to GPIO21
LED6	Red	Connected to RESET_OUT_N

4.7.5 Oscillators and clock input

Figure 4-9 shows the oscillator and clock scheme for the GR716B. The GR716B is by default feed by an external 25MHz crystal, GR716B's internal oscillator generates a clock signal out on pin XO_OUT which is connected back to the system clock, SYS_CLK. There is also an 25MHz oscillator on the board that can be connected to SYS_CLK by a not mounted resistor as alternative use. The SpaceWire clock is derived from a 200 MHz onboard oscillator. The user has a flexibility for the internal clocks on the chip; the internal system clock can either be derived directly from the SYS_CLK pin or generated using the PLL which is feed with the SPW_CLK. For more details of the internal PLL structure, clock gating and multiplexing features of the GR716B refer to User Manual [RD1]. The ETH0_RXCLK and ETH0_TXCLK frequency are 25MHz and derived from the Ethernet PHY. The PHY uses an 25MHz crystal. SPIM_SCK is an output signal from the GR716B and connected to an external SPI memory.

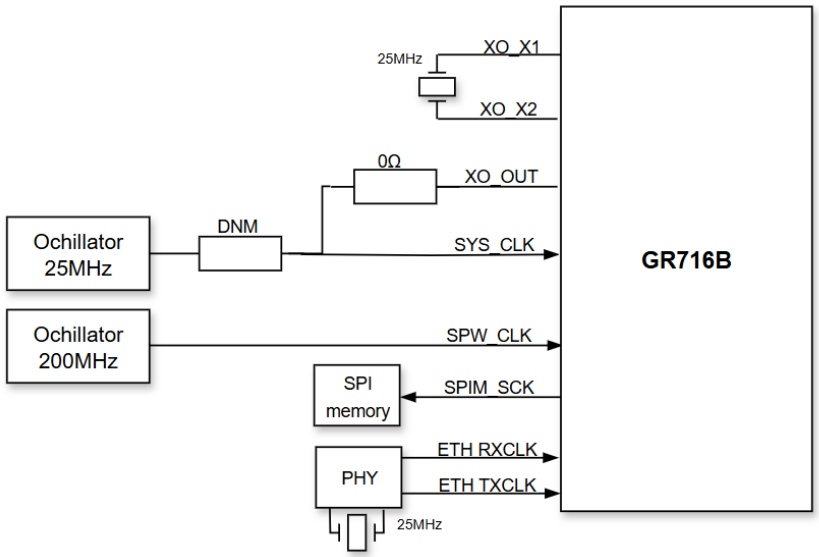

Figure 4-9 GR716B Clock Distribution *scheme*

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4.7.6 SpaceWire

The GR716B provides a SpaceWire router with two SpaceWire ports, where SpaceWire port [0] is connected to the FPGA and [1] is connected to the FMC+ connector. Since the LVDS signals has dedicate pins on the BGA package there is no need for internal multiplexing the signals, the pinout is shown in Figure 4-10. The GR716B does not provides an internal 100Ω termination and therefore this is added to the receiver signals on the board. All LVDS signals are routed in the PCB layout as point-to-point with an impedance of 100 Ω. Note that the LVDS pins needs to be configured appropriately.

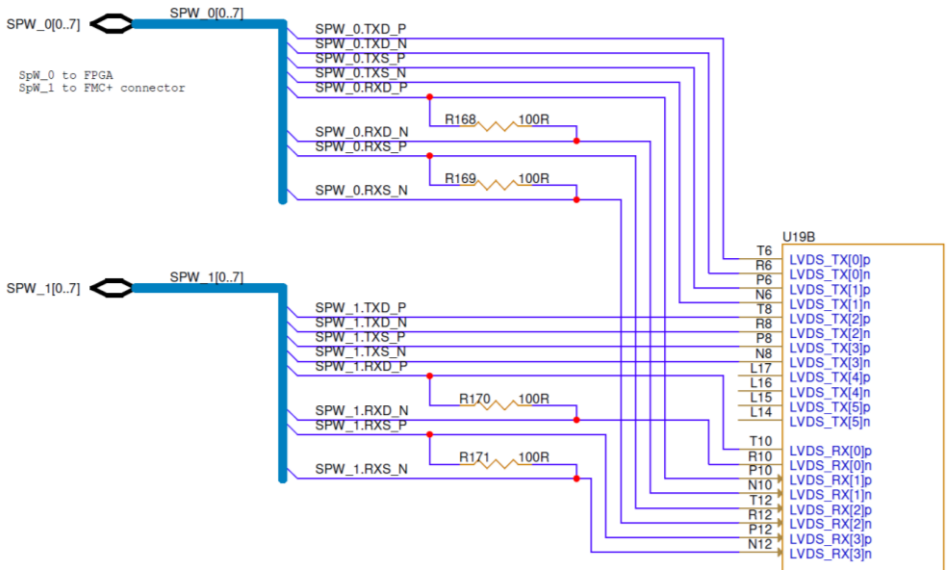

Figure 4-10 SpaceWire Implementation on the GR716B

4.7.7 FPGA

On the board GPIO13- GPIO17 from the GR716B are connected to the FPGA through a MUX. As default these are connected to usual GPIO pins to the FPGA, if changing the multiplexer, the signals will be connected to the configuration's pins on the FPGA. For more information about the configuration and programming the FPGA is described in section *4.8.1 - Configurate and programming.*

4.7.8 ADC

GR716B have in total 16 GPIO pins that can be used as ADC inputs. The GR716B-MIDI provides access to 12 of these GPIO pins.

The GR716B-MIDI board provides two MMCX connector (J7, J8) connected to GPIO39 and GPIO40 and an on-board thermistor connected to GPIO44. The thermistor (KR502F0J) is a NTC with a tolerance at 5 %. The ADC inputs GPIO37, GPIO38, GPIO41 to GPIO43 and GPIO55 to GPIO58 are accessible via the FMC+ connector. GPIO41 and GPIO42 are equipped with filter capacitors on the board to reduce disturbances. GPIO55 to GPIO58 are shared with the Ethernet interface via a MUX on the board. The nominal measurement range is 2.5V for single ended measurements and +/-2V for differential measurements. Figure 4-11 shows the implementation of the external ADC parts.

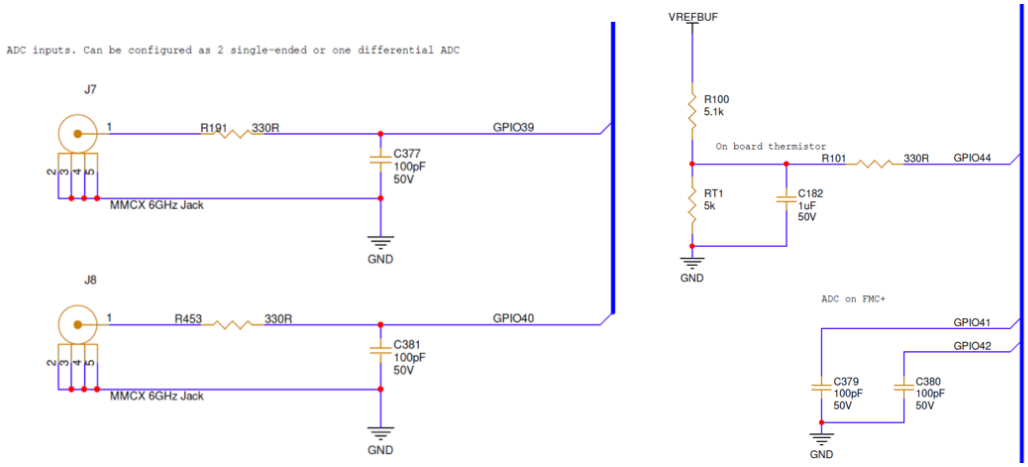

Figure 4-11 ADC implementation

4.7.9 DAC

GPIO47 and GPIO48 can be used as DAC outputs. On the GR716B-MIDI board there is one MMCX (J9) connected to GPIO48 together with a filter capacitor and 470 Ω resistor to ground. This set the maximum output voltage from the DAC to 1.88V. The GPIO47 is connected to the FMC+ connector together with a filter capacitor. To be able to use GPIO47 as DAC, a resistor needs to be placed to ground on a mezzanine board connected to the FMC+ connector. Note that both the mentioned signals (DAC) are multiplexed with the ethernet interface on the board, refer to section *4.7.12 Ethernet* for more details.

4.7.10 MRAM

In the BGA version of the GR716B component the memory interface has its own dedicated memory pins and therefore not needs to be multiplexed. The memory is allocated at address 0x50000000 and is controlled by mctrl1.

The implemented MRAM (AS3064316-045nX0IBCY) have a size of 64Mb (organized as 4M x 16 bit). The MRAM (Magneto resistive Random Access Memory) memory is a non-volatility memory with SRAM compatible read/write timing.

Figure 4-12 shows the implementation for the MRAM.

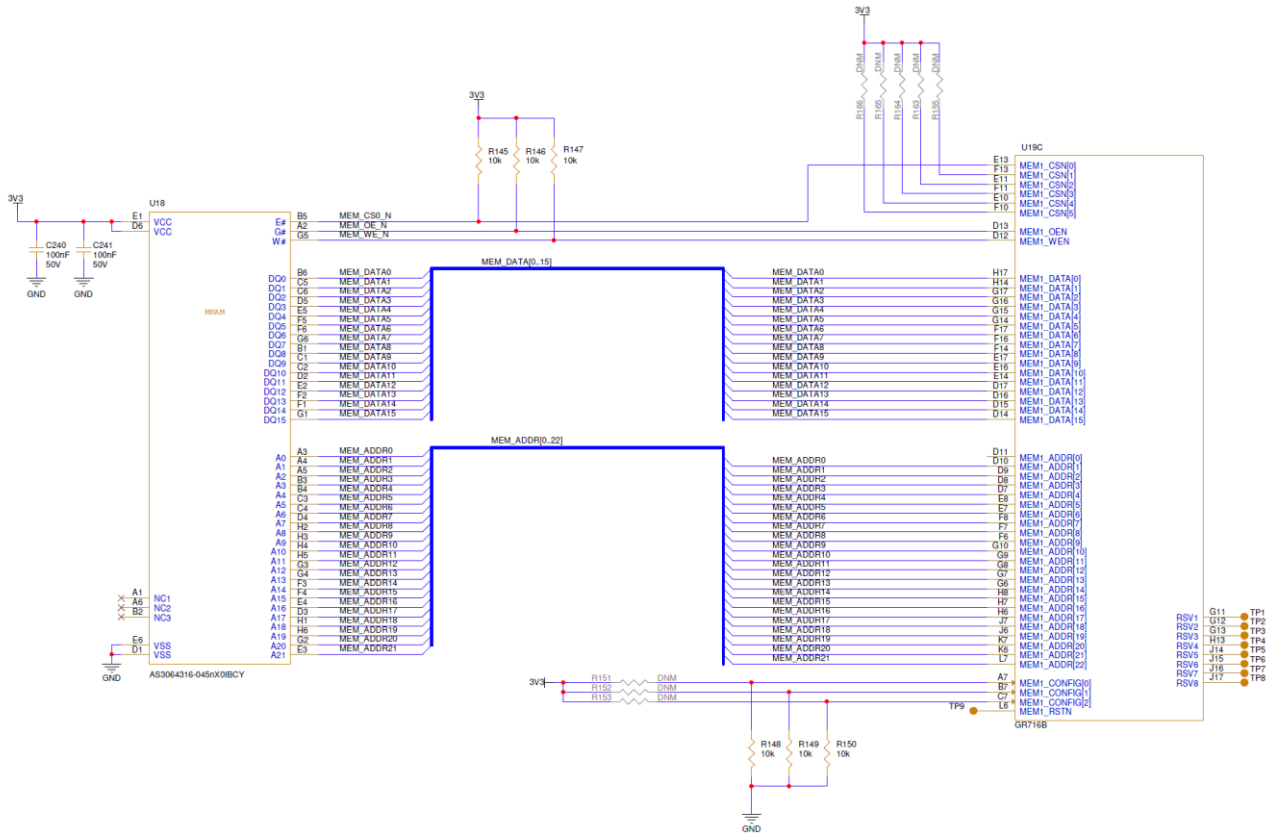

Figure 4-12 Implementation for MRAM

4.7.11 SPI memory

GR716B have two SPI memory controller, one that has dedicated pins, and the other one is connected to the multiplexed IO. On the GR716B-MIDI board a 512Mb SPI memory is implemented to the dedicated SPI memory pins. The used Serial NOR Flash memory (MX25L51245GZ2I-08G) provides 512Mb of non-volatile storage. The device supports one, two or four I/O modes.

This device can be used for program storage or as a boot device for the board.

4.7.12 Ethernet

The GR716B Microprocessor supporting ethernet in 10 or 100 Mbit/s. Since the ethernet interfaces is pin-multiplexed on the GR716B component, the GR716B-MIDI board provides an external multiplexer to be able to switch between the ethernet interface or to the other interfaces. These are connected to the FMC+ connector except one signal (GPIO48) that is connected to a MMCX connector and can be used as a DAC, see Figure 4-14. The board is as default in ethernet mode since the jumper (JP2) is not set.

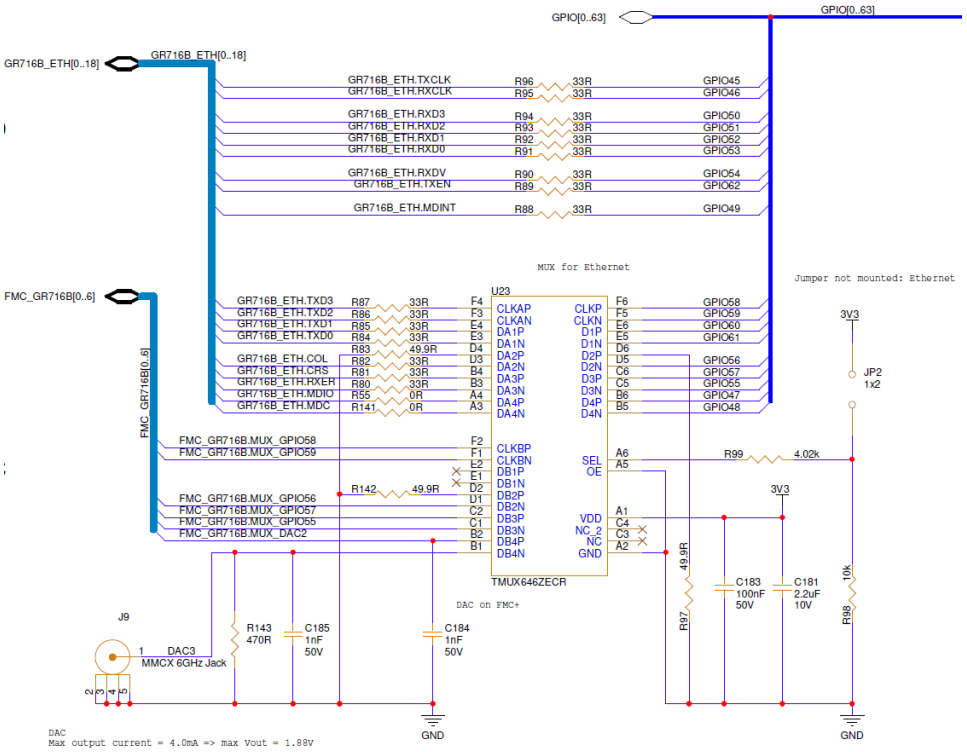

Figure 4-13 Ethernet – MUX

The Ethernet PHY (KSZ9031) that is implemented on the board supports 10/100 Mbit/s Ethernet see Figure 4-14. The Ethernet interface uses a RJ45 connector that has an integrated transformer. The PHY address is hard-wired to 1 (“001”). The transceiver uses a 25MHz oscillator.

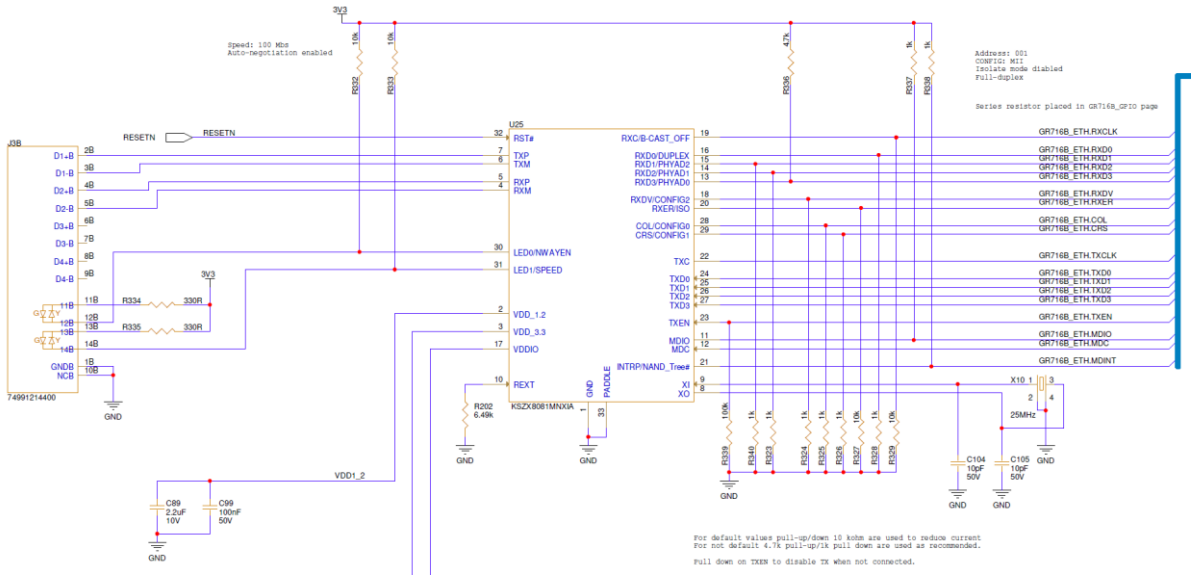

Figure 4-14 ETH implementation

4.8 CertusPro-NX FPGA

CertusPro-NX is a low-power general purpose FPGA and is built on the Lattice Nexus FPGA platform, using low-power 28 nm FD-SOI technology. In this design the LFCPNX-100-9BBG484 is used, which is the commercial-off-the-shelf (COTS) variant of the radiation-tolerant CertusPro-NX-RT FPGA. It provides a total of 100k logic cells and speed grade -9 (fastest) in a package size of 19x19mm, (ball-pitch of 0.8mm). For more information about the CertusPro-NX, see the corresponding data sheet [RD3].

The *GR716B-MIDI* board can be used to demonstrate features like ADC, SerDes, LVDS, Ethernet and the DDR3 DRAM interface for the CertusPro-NX see Figure 4-15. To integrate the FPGA with Gaisler IP, please see the webpage for more details;
https://www.gaisler.com/grlib-ip-library

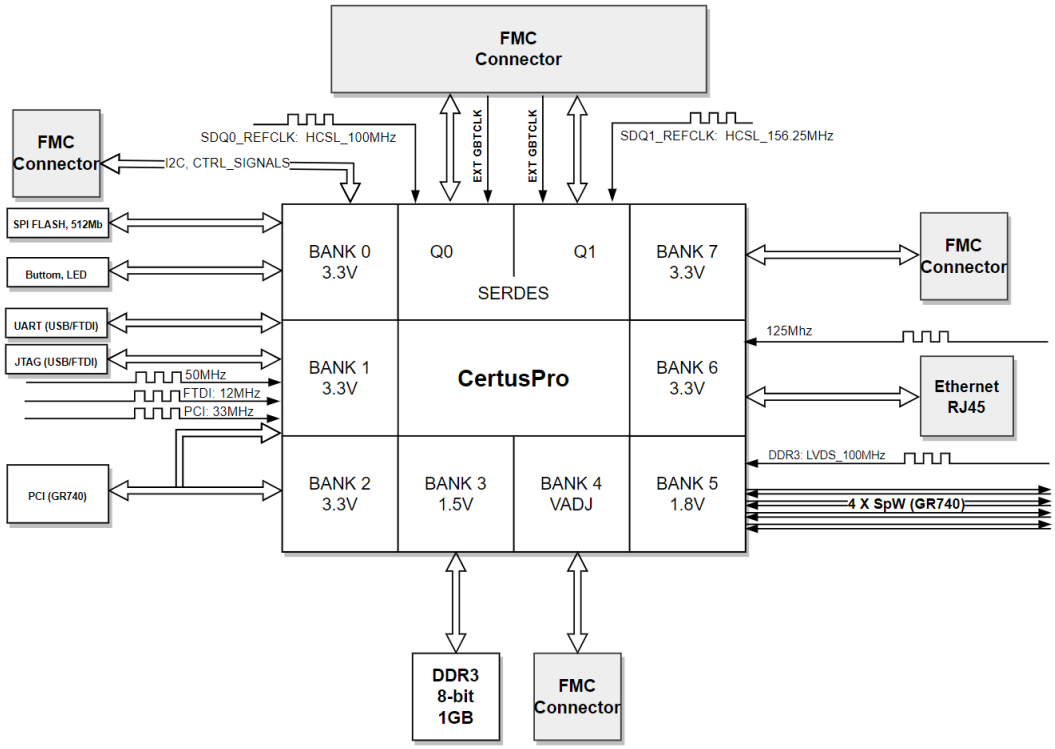

Figure 4-15 CertusPro-NX implementation

4.8.1 Configurate and programming

In this design there are three ways to program the FPGA, through the JTAG or SPI interface or through the external SPI flash memory. There is an on-board mux for switching between JTAG or SPI interface since they shared the same pins on the FPGA. The JTAG interface is connected to a FTDI chip and is accessible through the USB-C connector J2. The SPI interface is connected to the GR716B, note that the GR716B needs to be configurated accordantly. As default the MUX and the configuration state of the FPGA is in JTAG mode, the jumper (JP4) is not connected. For more information about the configuration and programming of the CertusPro-NX refer to the User Guide for Nexus Platform [RD4].

Figure 4-16 shows the block scheme of the FPGA programming, Figure 4-17 shows the implementation of the JTAG/SPI multiplexer.

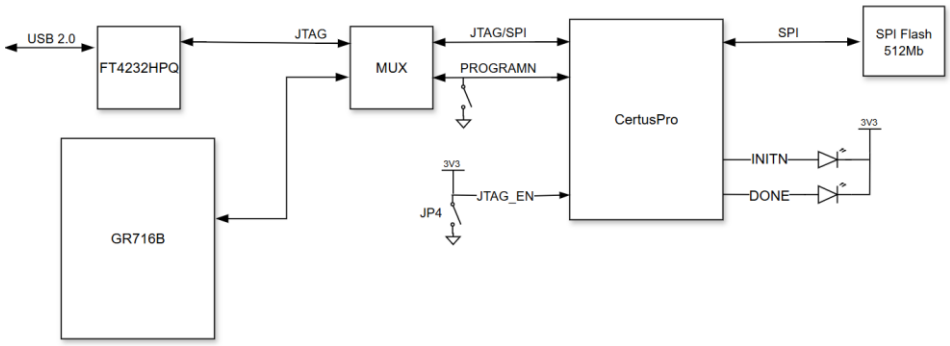

Figure 4-16 Programming the FPGA

There are four corresponding program signals.

1. PROGRAMN (input): Initiate configuration sequence when asserted LOW. This pulled up signal is connected to a switch (SW2) and jumper (JP3) for the user to set it to LOW activating configuration mode. The signals is connected to GR716B (GPIO16) if in SPI-mode. The signal can also be connected to pin BDBUS7 on the FTDI chip since there is one resistor that is not mounted.

2. INITN (Open Drain I/O pin): This signal is driven to LOW when configuration sequence is started, and the FPGA starts to load configuration data from the external SPI Flash.

3. DONE (Open Drain I/O pin): This signal indicate that the FPGA is in user mode. This signal is driven to LOW during configuration. It is released (high) to indicate completed configuration.

4. JTAG_EN (input): Is driven HIGH, can be set too low to disable JTAG with setting the jumper (JP4)

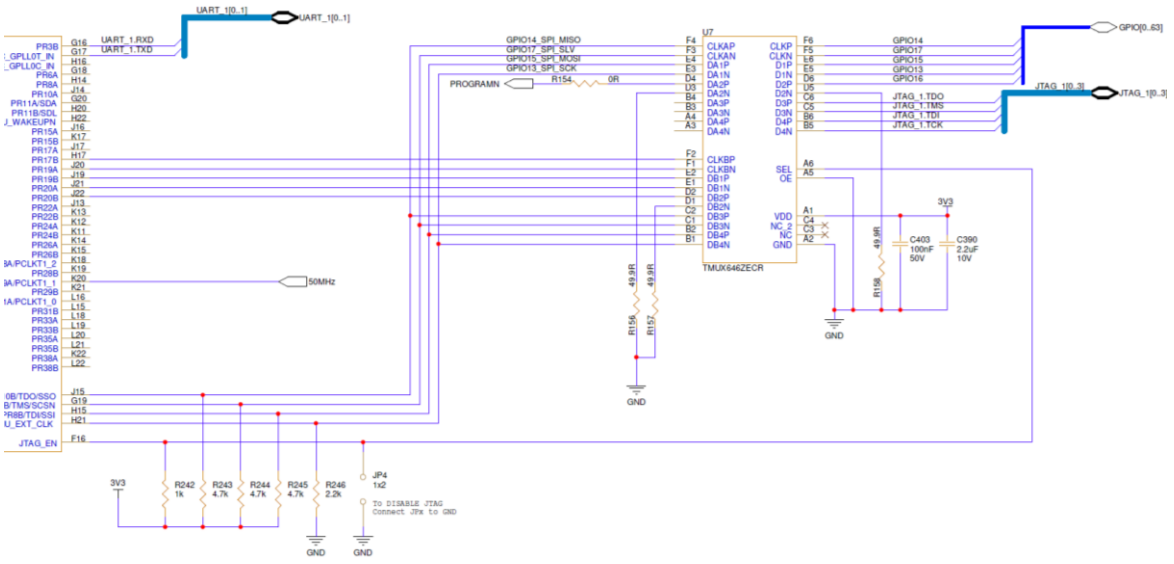

Figure 4-17 Implementation of the SPI/JTAG multiplexer

4.8.2 LED

On the board there are LEDs corresponds to the CertusPro-NX, see Table 4-7 for more information and Figure 4-18 for the board placement.

Table 4-7 LED correspond the CertusPro-NX

LED	Colour	Description
LED7	Red	Connected to INITN, indicates when errors occur during configuration
LED11	Green	Connected to DONE signal, indicates when configuration completed successfully
LED12	Green	Connected to GPIO
LED13	Green	Connected to GPIO
LED14	Green	Connected to GPIO
LED15	Green	Connected to GPIO

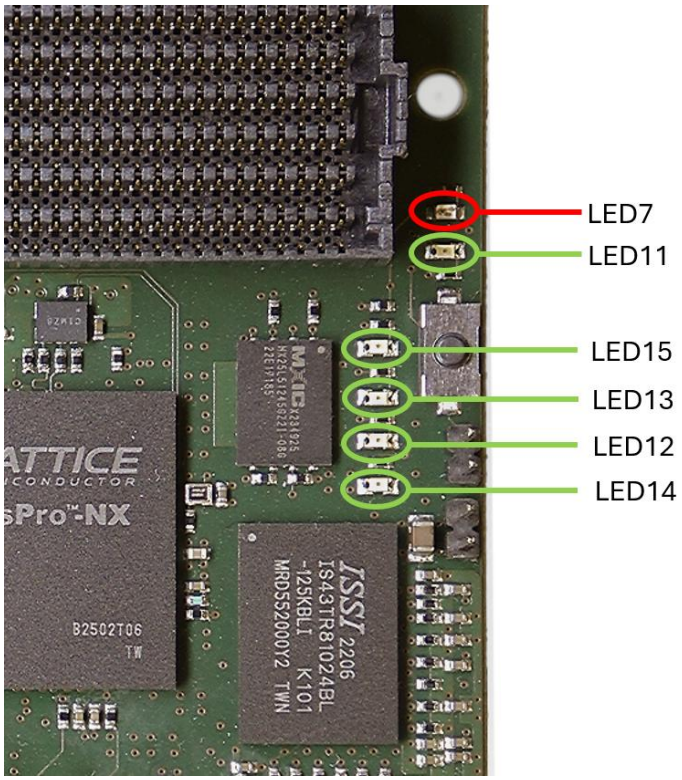

Figure 4-18 LED7 and LED(11-15) board placement

4.8.3 JTAG

The JTAG link is routed via J2 (USB-C) through the FTDI chip. The FPGA has dedicated JTAG pins. To enable the JTAG interface the signal JTAG_EN must be HIGH. In this design this signal has a pull-up resistor and is therefore HIGH by default. The interface can be disabled by install the jumper (JP4), connected to GND.

4.8.4 SPI FLASH

The used Serial NOR Flash memory (MX25L51245GZ2I-08G) provides 512Mb of non-volatile storage. The device supports one, two or four I/O modes. The Flash memory is connected to the dedicated system configuration (sysCONFIG) pins on the FPGA and implemented as four I/O mode see Figure 4-19.

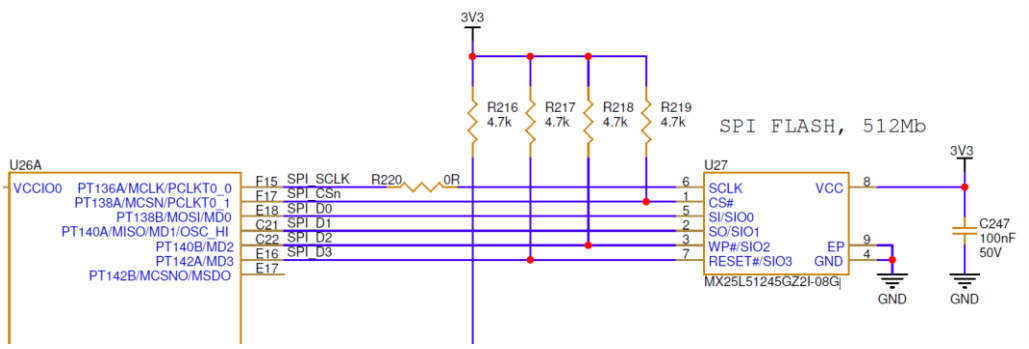

Figure 4-19 SPI Flash implementation

4.8.5 Oscillators and clocks input

Multiples clocks are providing inputs to have a flexible development environment. All clocks are to a dedicated clock input pin on different banks. Each clock input can be set to the reference clock to the global PLL. The PLL can divide the frequency by ÷2, ÷4, ÷8, ÷16, ÷32, ÷64, ÷128, and ÷1 (bypass). For more information about the clocking structure of the CertusPro-NX, please refer to [RD3].

Figure 4-20 shows the clock scheme for the FPGA.

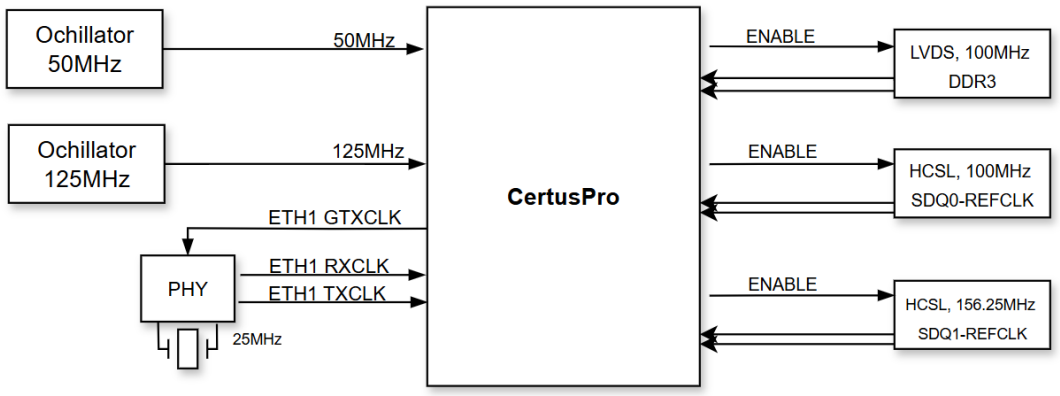

Figure 4-20 CertusPro-NX Clock Distribution scheme

The clock signals 50MHz and 125MHz is derived from onboard oscillators. In MII mode the ETH1_GTXCLK is not used. The ETH1_RXCLK and ETH1_TXCLK are 25MHz and derived from the Ethernet PHY. In GMII mode the ETH1_GTXCLK is used and set to 125MHz. The ETH1_RXCLK is running at 25MHz and derived from the Ethernet PHY. The Ethernet PHY uses an external crystal of 25MHz.

The clock oscillator that is aimed for the DDR3 interface is of LVDS type with a frequency of 100MHz and is connected to dedicated differential clock pair.

The two SerDes quads, Q0 and Q1 have one reference clock each (on the board) 100MHz and 156.25MHz, for more information about the SerDes quad see section *4.8.10 SerDes*. The two-clock reference that are on the board are of HCSL type and is by default disabled.

4.8.6 SpaceWire

There are one SpaceWire channel between the GR716B and the CertusPro-NX. The SpaceWire signals are implemented as LVDS on bank 5 in the FPGA and is supplied with 1V8, see Figure 4-21 for the pinout. The CertusPro-NX provides an on chip programmable termination so there is no need for external resistor on the receiving signals. All LVDS signals are routed in the PCB layout as point-to-point with an impedance of 100 Ω.

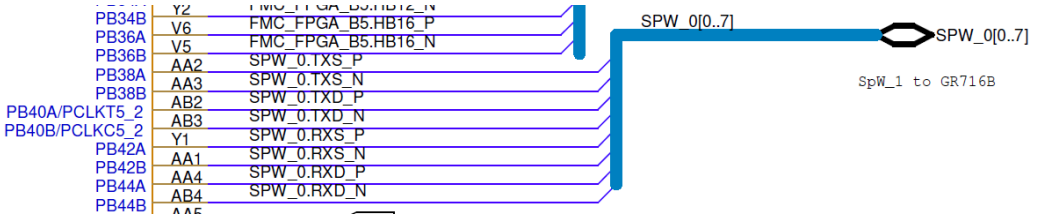

Figure 4-21 SpaceWire Implementation on the FPGA

4.8.7 DDR3 Memory

The design has a DDR3 memory interface connected to bank 3 supporting DQS logic. The bank is powered with 1V5.The used DDR3 memory (S43TR81024BL-125KBLI) provides 1GB volatile storage organized as 1G x 8 and have a JEDEC Speed grade DDR3-1600K. The implementation is shown in Figure 4-22. There are pins on the FPGA dedicated for the DDR3 operation and they are divided into DQS groups. One DQS group includes DQS, DQS#, eight DQ and one DM. A voltage reference pin is also needed for the implementation. For more information about the DDR3 interface please refer to [RD5].

To achieve correct termination and power supplies requirements, an external power management IC (TPS51206) is used.

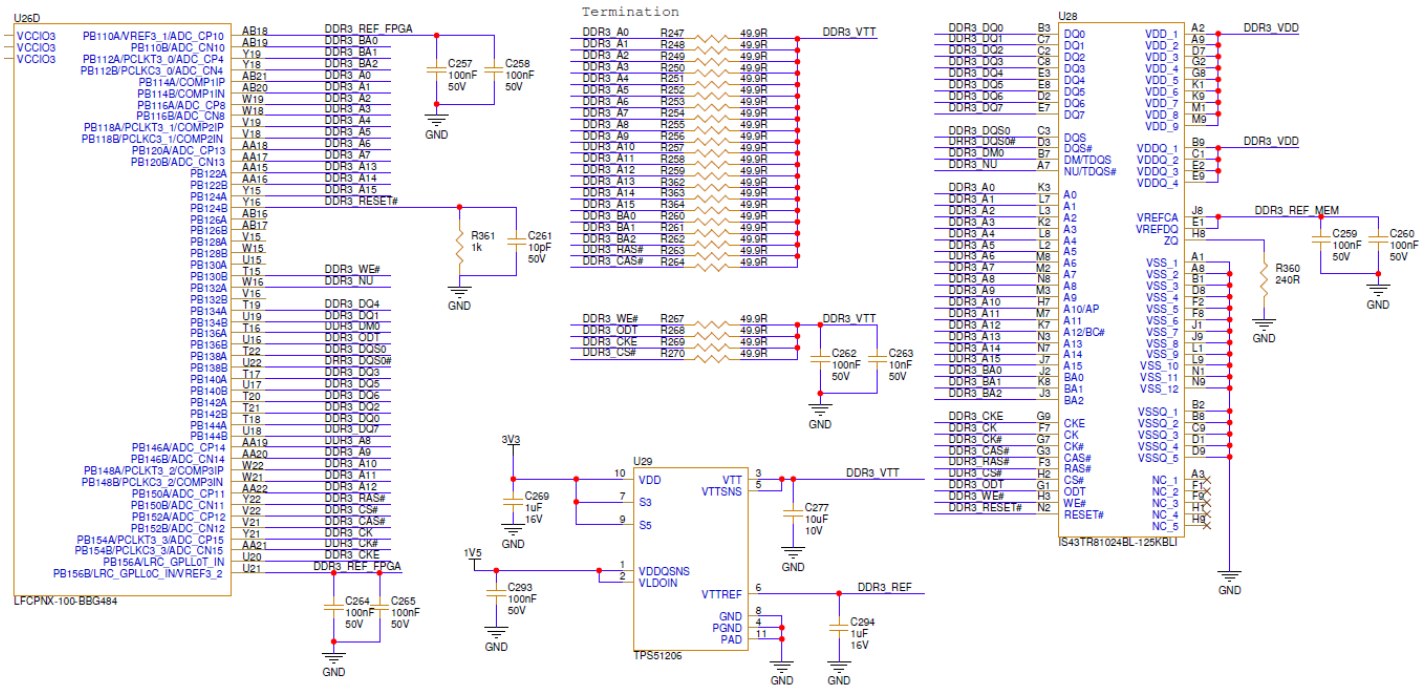

Figure 4-22 CertusPro-NX DDR3 memory implementation

4.8.8 Ethernet

The Ethernet interface is implemented on bank 6 using a 3V3 supply. Figure 4-23 shows the implementation for the interface. The RJ45 connector that is used has an integrated transformer. The Ethernet PHY transceiver that is used (KSZ9031) supports 10/100/1000Mbit/s Ethernet. PHY address is hard-wired to 2 (“010”). The transceiver uses an external 25MHz oscillator. Different clock configuration is used depending on which ethernet mode that is selected, se section *4.8.5* for more information.

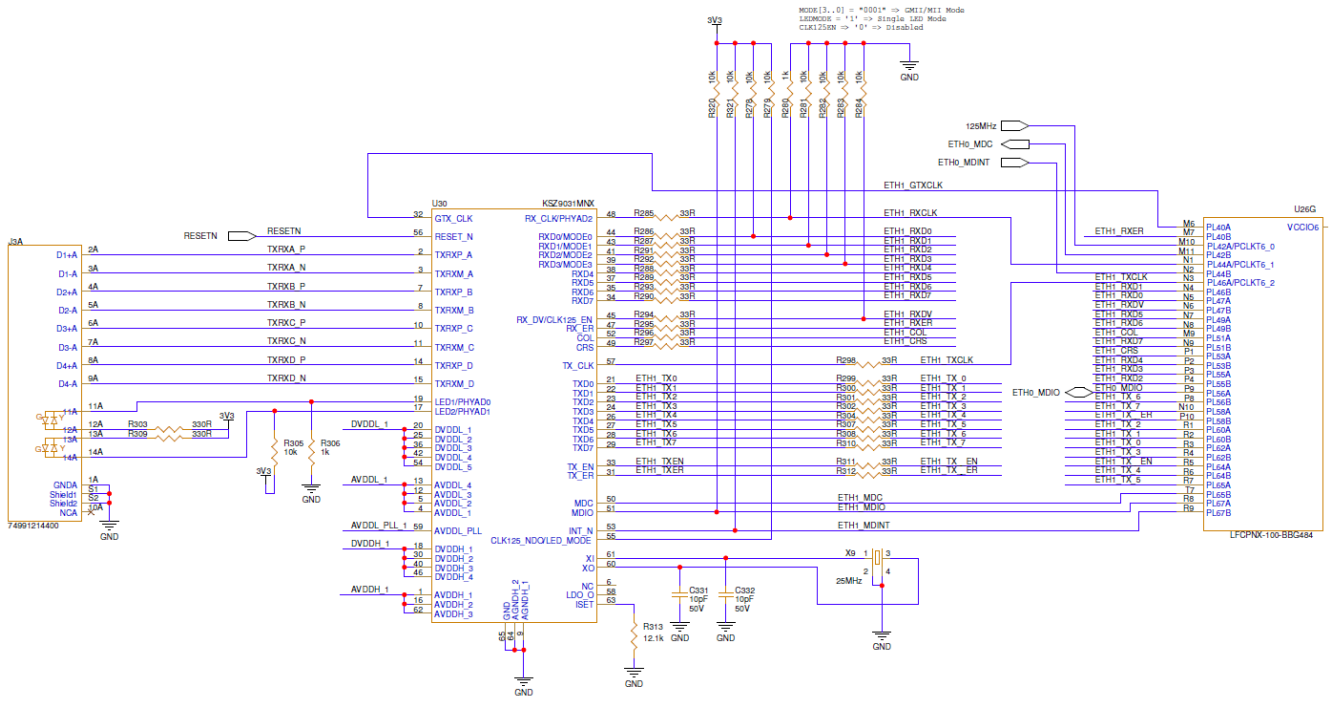

Figure 4-23 Ethernet implementation

4.8.9 ADC

On the GR716B-MIDI board here are four MMCX connector connected to the FPGA, where two (J5, J6) is connected the dedicated ADC block as two single ended and the other two (J10, J11) are connected to bank 5. The reference voltage (VREF) to the ADC block is taken from the GR716B. The reference voltage is divided down to 1.74V. This is also the maximum single ended input voltage to the ADC.

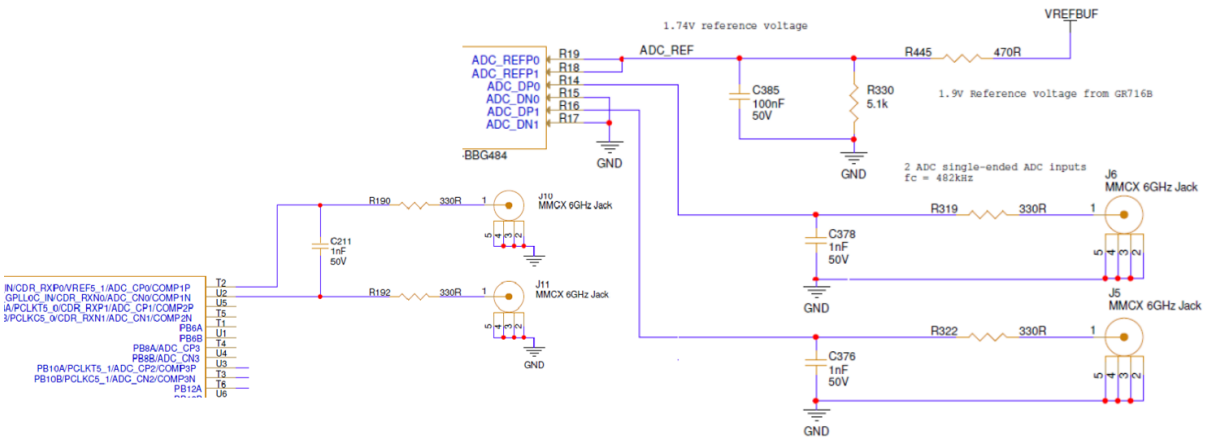

Figure 4-24 ADC implementation

4.8.10 SerDes

The CertusPro-NX provide two quads (Q0, Q1) with four SerDes channels and two reference clocks each. In this design both quads are used with two SerDes channels and both reference clocks, see Figure 4-25 for the SerDes implementation. All the SerDes channels and the external reference clocks are connected to the FMC+ connector, refer to section *4.9* for the signals and pinout. The reference clocks on the board are HCSL type of 156.25MHz for Q0 and 100MHz for Q1. R314 -R317 sets the termination impedance, and it is set to 1.15kΩ which results in (RDIFF=) 100Ω. All corresponding differential signals for the SerDes are routed in the PCB layout with an impedance of 100Ω.

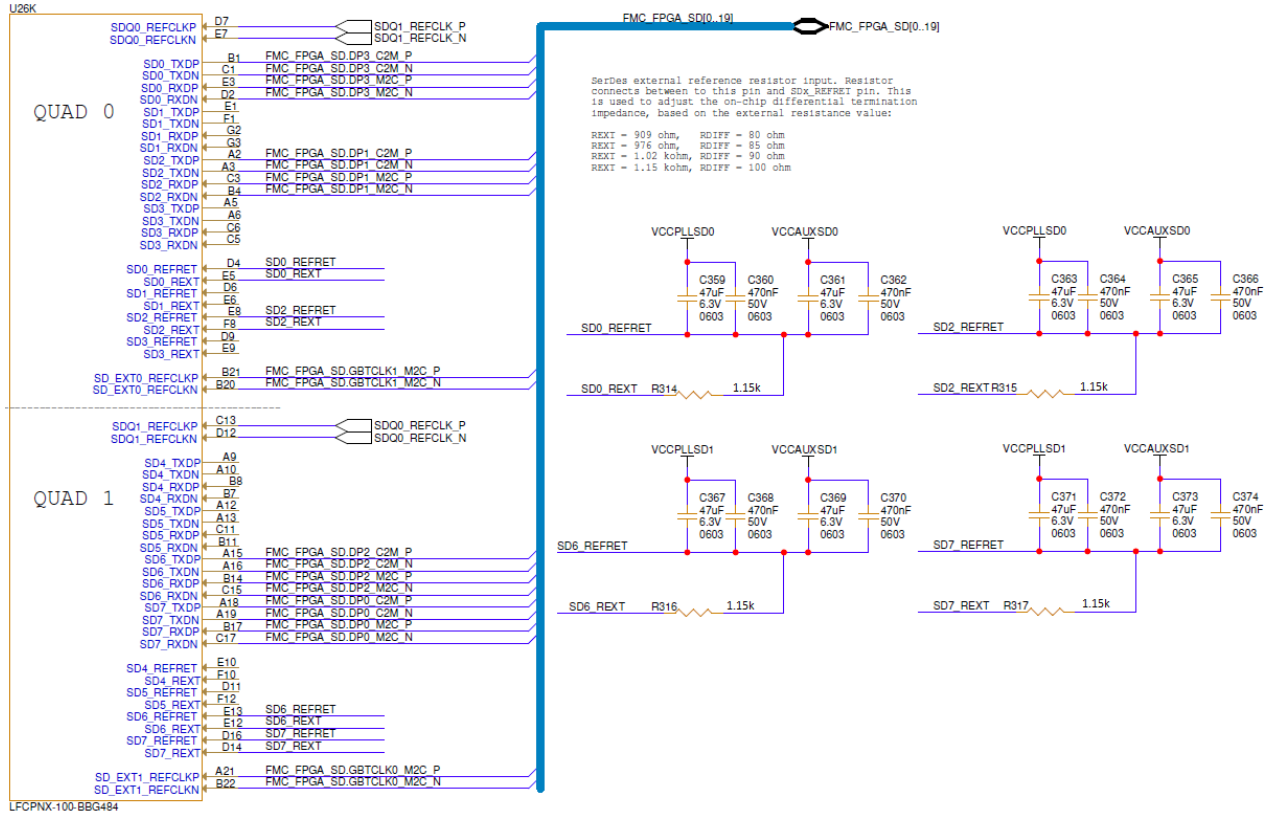

Figure 4-25 SerDes implementation

4.9 FMC+ connector

The *GR716B-MIDI* is equipped with an FMC+ connector (FPGA Mezzanine Card), that is connected to both the GR716B and CertusPro-NX, see Figure 4-26. The FMC+ connector is divided into two section, Low Pin Count (LPC) and High Pin Count (HPC) and is described for the two devices below:

1. CertusPro-NX: Bank 4 is connected to LVDS signals on the LPC part and have an adjustable voltage, default it is set to 1.8V (it must not exceed 1.8V). Bank 5 is supplied with 1V8 and connected to the HPC section. Bank 7 is supplied with 3V3 and is connected to the HPC. CertusPro-NX contains two quads of four SerDes channels. In this design the first quad Q0, is connected to the SerDes channel (DP0) and a reference clock (GBTCLK0) in LPC and to the SerDes channel (DP2) in HPC. The second quad Q1 is connected to SerDes channels (DP1 & DP2) and reference clock (GBTCLK1) in the HPC

2. GR716B: SpaceWire router port 2 and GPIO signals are connected to the HPC part of the FMC+ connector.

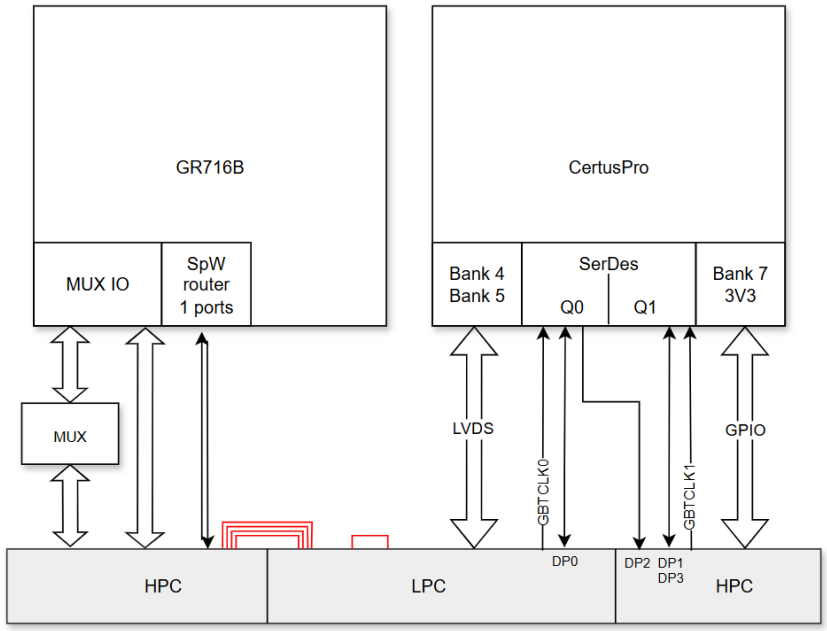

Figure 4-26 FMC+ connector scheme

NOTE: Some signals are connected to two different FMC connector pins, which is illustrated in Figure 4-26 in red, each line represents a differential pair. Due do this it is **IMPORTANT** to check the connection to the mezzanine card before connecting with the *GR716B-MINI* board, see Appendix C and Table 4-8.

To avoid damage to the SPW interfaces due to common mode voltage the following actions should be performed before the equipment's that will be connected by SpaceWire are powered on.

● Before connecting any SpaceWire cables, make sure that there is no voltage difference between the different equipment grounds. E.g., measure the voltage between the different equipment grounds with a voltmeter. The result should be close to 0 V.

● After the SpaceWire cables are connected, make sure that the equipment grounds are low ohmic connected to each other. E.g., measure the resistance between the different equipment grounds with a multimeter in resistance mode. The result should be less than 1 Ω

This board is intendent to be used together with a mezzanine board. See the user's manual of the mezzanine board for information about the connection and grounding of the SpaceWire interface. Users using the board stand alone or design their own mezzanine board must ensure that equipment's connected via SPW have grounds that are connected.

Table 4-8 list all signals for the FMC+ connector is listed.

Note: In the column “comments” a notification is done whether the signal is connected to two different FMC connector pins (s.a *(FMC+) JX.NXX*) or other usage

Table 4-8 Pinout for FMC+ connector

Pin FMC	Signal Name	CertusPro-NX Bank	CertusPro-NX Pin	GR716B pin	Comment
LPC					
C2	DP0_C2M_P	Q1	A18		
C3	DP0_C2M_N	Q1	A19		
C6	DP0_M2C_P	Q1	B17		
C7	DP0_M2C_N	Q1	C17		
C10	LA06_P	4	W7		
C11	LA06_N	4	Y7		
C14	LA10_P	4	T8		
C15	LA10_N	4	U8		
C18	LA14_P	4	V7		
C19	LA14_N	4	U7		
C22	LA18_CC_P	4	AA7		
C23	LA18_CC_N	4	Y8		
C30	FMC_SCL	0	F18		
C31	FMC_SDA	0	G21		
C34	GA0				GND
C39	3PV3				
D1	FMC_PG_C2M	0	D22		
D4	GBTCLK0_M2C_P	Q1	A21		
D5	GBTCLK0_M2C_N	Q1	B22		
D8	LA01_CC_P	4	AB7		
D9	LA01_CC_N	4	AB8		
D14	LA09_P	4	W8		
D15	LA09_N	4	V8		
D17	LA13_P	4	AA8		
D18	LA13_N	4	AA9		
D20	LA17_CC_P	LA23_P			(FMC+) J4.D23
D21	LA17_CC_N	LA23_N			(FMC+) J4.D24
D23	LA23_P	4	U9		(FMC+) J4.D20
D24	LA23_N	4	T9		(FMC+) J4.D21
D26	LA26_P	4	AA14		(FMC+) J4.F25
D27	LA26_N	4	Y14		(FMC+) J4.F26
D32	3P3VAUX				
D35	GA1				GND
D36	3PV3				
D38	3PV3				
D40	3PV3				
G6	LA00_CC_P	4	AB9		
G7	LA00_CC_N	4	AB10		
G9	LA03_P	4	U10		
G10	LA03_N	4	T10		
G12	LA08_P	4	AA10		
G13	LA08_N	4	Y10		
G15	LA12_P	4	W10		
G16	LA12_N	4	V10		
G18	LA16_P	4	U11		(FMC+) J4.K37
G19	LA16_N	4	V11		(FMC+) J4.K38
G24	LA22_P	4	AB11		

G25	LA22_N	4	AB12		
G27	LA25_P	4	Y11		
G28	LA25_N	4	W11		
G39	VADJ				
H1	VREF_A_M2C	4	T14		
H2	PRSNT_M2C_L	0	E22		
H4	CLK0_M2C_P	4	U12		(FMC+) J4.K25
H5	CLK0_M2C_N	4	T12		(FMC+) J4.K26
H7	LA02_P	4	Y13		(FMC+) J4.K28
H8	LA02_N	4	W13		(FMC+) J4.K29
H10	LA04_P	4	V14		
H11	LA04_N	4	W14		
H13	LA07_P	4	AA11		
H14	LA07_N	4	AA12		
H16	LA11_P	4	AB13		
H17	LA11_N	4	AA13		
H19	LA15_P	4	AB14		
H20	LA15_N	4	AB15		
H25	LA21_P	4	V13		
H26	LA21_N	4	U13		
H40	VADJ				
HPC					
A2	DP1_M2C_P	Q0	C3		
A3	DP1_M2C_N	Q0	B4		
A6	DP2_M2C_P	Q1	B14		
A7	DP2_M2C_N	Q1	C15		
A10	DP3_M2C_P	Q0	E3		
A11	DP3_M2C_N	Q0	D2		
A14	GPIO29			A11	
A15	GPIO30			B11	
A18	GPIO33			C10	
A19	GPIO34			A9	
A22	DP1_C2M_P	Q0	A2		
A23	DP1_C2M_N	Q0	A3		
A26	DP2_C2M_P	Q1	A15		
A27	DP2_C2M_N	Q1	A16		
A30	DP3_C2M_P	Q0	B1		
A31	DP3_C2M_N	Q0	C1		
A34	MUX_GPIO55			R18	MUX:ed on board
A35	MUX_GPIO56			P19	MUX:ed on board
A38	GPIO41			N2	Capacitor added on board
A39	GPIO42			P1	Capacitor added on board
B1	CLK_DIR	0	E21		
B4	GPIO0			J19	
B5	GPIO1			J18	
B8	GPIO2			H20	
B9	GPIO3			G20	
B12	GPIO27			C13	
B13	GPIO28			A12	
B16	GPIO31			A10	
B17	GPIO32			B10	
B20	GBTCLK1_M2C_P	Q0	B21		
B21	GBTCLK1_M2C_N	Q0	B20		
B24	GPIO25			A13	
B25	GPIO26			B13	
B28	GPIO35			A8	
B29	GPIO36			C8	

B32	GPIO37			K1	
B33	GPIO38			L2	
B36	MUX_DAC2			Y6	MUX:ed on board, Capacitor added on board
B37	GPIO43			P3	
F1	PG_M2C	0	F20		
F04	HA00_CC_P	7	L9		
F05	HA00_CC_N	7	M8		
F07	HA04_P	7	L5		
F08	HA04_N	7	L4		
F10	HA08_P	7	J9		
F11	HA08_N	7	J8		
F13	HA12_P	7	M2		
F14	HA12_N	7	M3		
F19	GPIO22			A14	
F29	MUX_GPIO59			L19	MUX:ed on board
F22	HB02_P	5	V1		
F23	HB02_N	5	W1		
F25	HB04_P	LA26_P	-		(FMC+) J4.D26
F26	HB04_N	LA26_N	-		(FMC+) J4.D27
F28	HB08_P	5	W6		
F29	HB08_N	5	W2		
F31	HB12_P	5	W2		
F32	HB12_N	5	Y2		
F34	HB16_P	5	V6		
F35	HB16_N	5	V5		
F37	FMC_GR716B.MUX_GPIO57			N20	MUX:ed on board
F38	FMC_GR716B.MUX_GPIO58			N18	MUX:ed on board
F40	VADJ				
K07	HA02_P	7	H1		
K08	HA02_N	7	J1		
K10	HA06_P	7	H8		
K11	HA06_N	7	H7		
K13	HA10_P	7	L11		
K14	HA10_N	7	L10		
K17	GPIO4			G19	
K19	GPIO7			F18	
K20	GPIO8			E20	
K22	GPIO11			D18	
K23	GPIO12			C20	
K25	HB00_CC_P	LA15_P			(FMC+) J4.H4
K26	HB00_CC_N	LA15_N			(FMC+) J4.H5
K28	HB06_CC_P	LA11_P			(FMC+) J4.H7
K29	HB06_CC_N	LA11_N			(FMC+) J4.H8
K31	HB10_P	5	W3		
K32	HB10_N	5	Y3		
K34	HB14_P	5	W5		
K35	HB14_N	5	Y5		
K37	HB17_CC_P	LA07_P			(FMC+) J4.H18
K38	HB17_CC_N	LA07_N			(FMC+) J4.H19
E2	HA01_CC_P	7	K10		
E3	HA01_CC_N	7	K9		
E6	HA05_P	7	K6		
E7	HA05_N	7	L6		
E9	HA09_P	7	K4		
E10	HA09_N	7	K3		
E12	HA13_P	7	L1		

E13	HA13_N	7	M1		
E15	GPIO18			A16	
E16	GPIO19			B16	
E18	GPIO23			B14	
E19	GPIO24			C14	
E21	SPW_1.TXS_P			P8	
E22	SPW_1.TXS_N			N8	
E24	SPW_1.TXD_P			T8	
E25	SPW_1.TXD_N			R8	
E27	SPW_1.RXS_P			P12	
E28	SPW_1.RXS_N			N12	
E30	SPW_1.RXD_P			T10	
E31	SPW_1.RXD_N			R10	
E33	FMC_FPGA_B5.HB19_P	5	U3		
E34	FMC_FPGA_B5.HB19_N	5	T3		
E36	FMC_FPGA_B5.HB21_P	5	T6		
E37	FMC_FPGA_B5.HB21_N	5	U6		
E39	VADJ				
J6	HA03_P	7	L8		
J7	HA03_N	7	K8		
J9	HA07_P	7	L3		
J10	HA07_N	7	L2		
J12	HA11_P	7	J7		
J13	HA11_N	7	J6		
J15	HA14_P	7	M4		
J16	HA14_N	7	M5		
J18	GPIO5			F20	
J19	GPIO6			F19	
J21	GPIO9			D20	
J22	GPIO10			D19	

REVISION INFORMATION

Issue	Date	Section / Page	Description
1.0	2026-06-12		First release of this document

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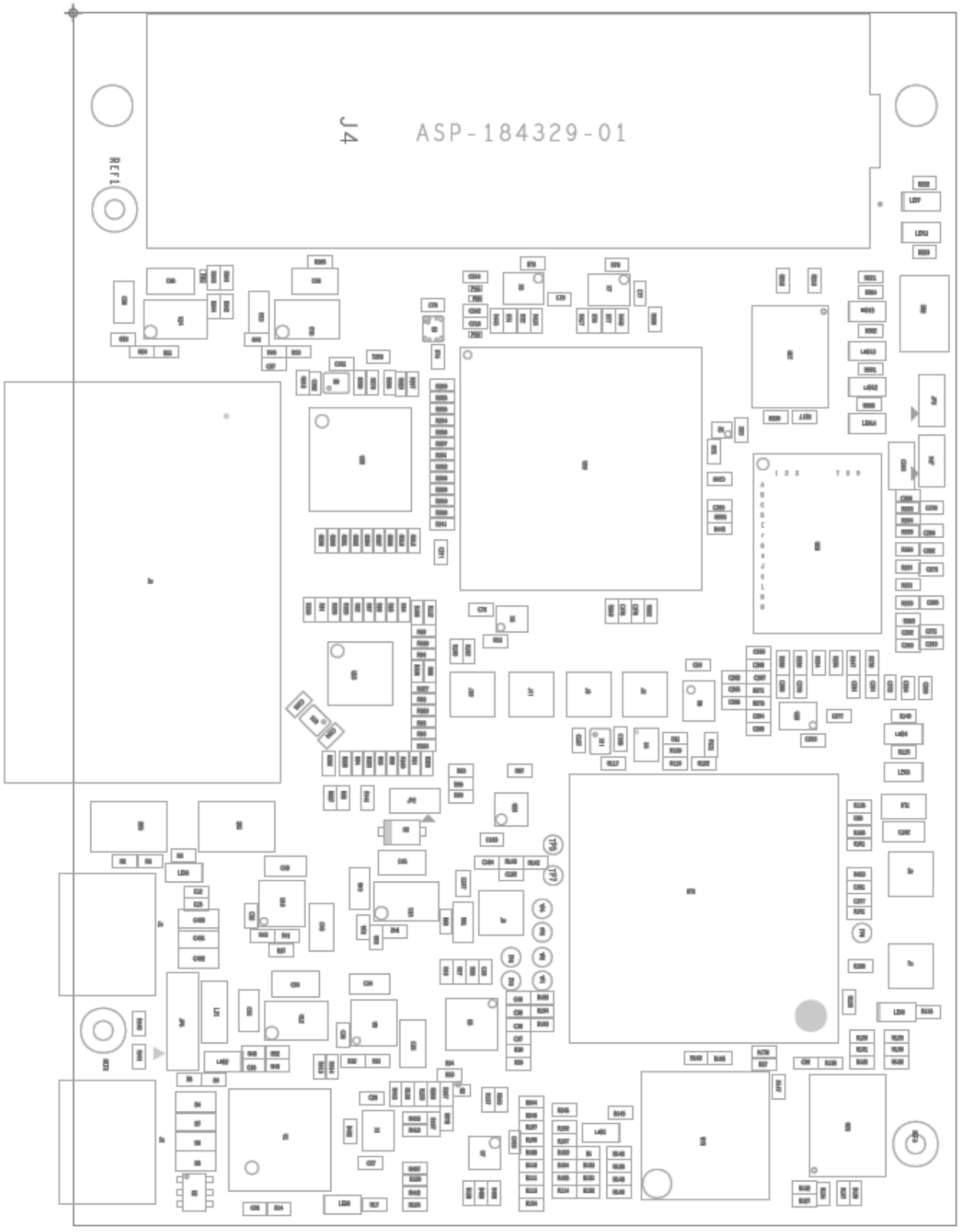
APPENDIX A



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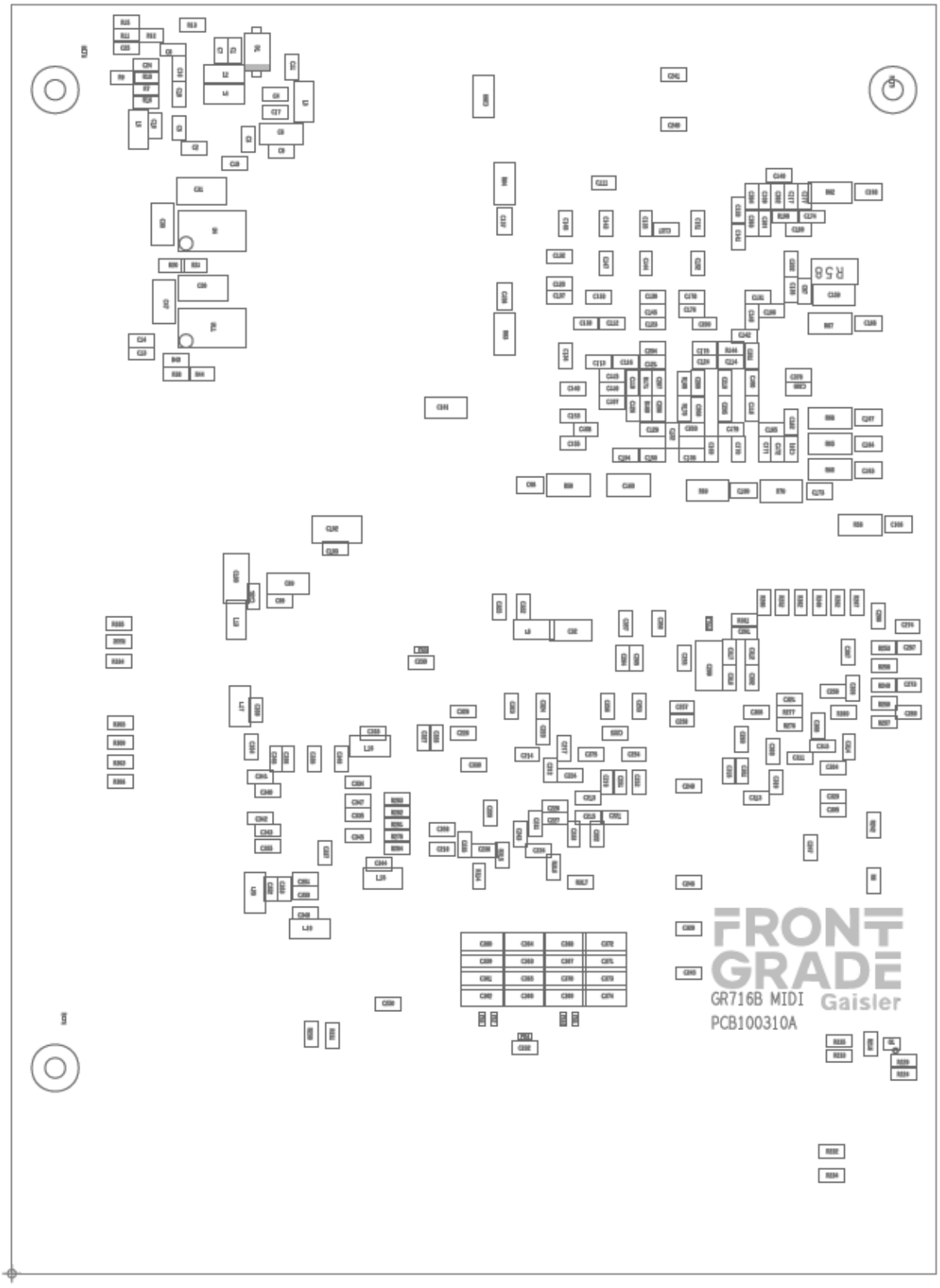
APPENDIX B



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APPENDIX C