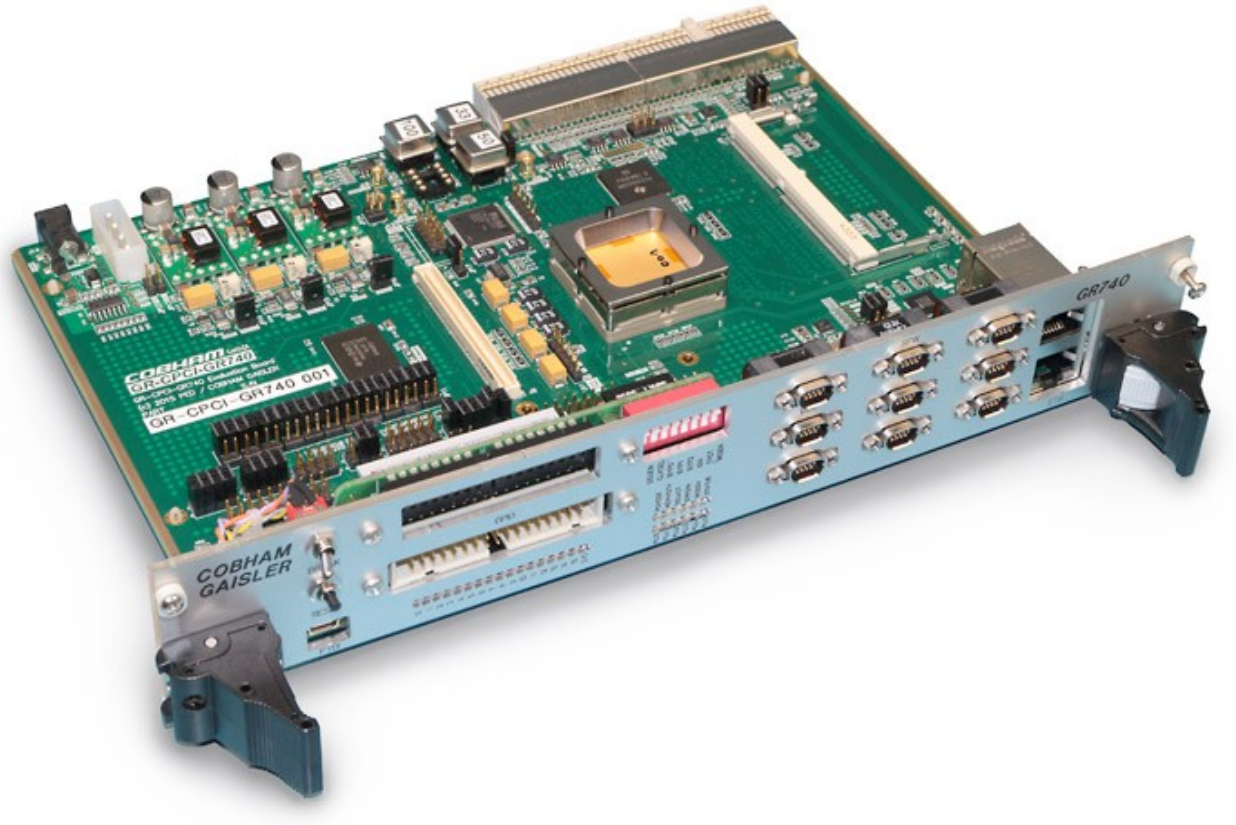
GR740 Technical Note on Benchmarking and Validation



Technical Note

Doc. No GR740-VALT-0010

Issue 3.4

2019-04-24

CHANGE RECORD

Issue	Date	Section / Page	Description
2.0	2016-12-28	All	First public release
2.1	2017-01-11	All 1.1 4.4 5 6	Remove contract number and deliverable information from first page and footers Minor updates to Scope Updated SpW transfer rate Added new SpW and Ethernet power measurements. Updated text. Added statements on SEL and TID performance.
2.2	2017-01-25	4.2 4.4 5	Update PARSEC and EEMBC Multibench results. Updated with PCI transfer rate. Corrected LVDS and IO power in scenario 1.
3.0	2018-08-22	1.1 1.2 2 4.1, 4.3, 4.4, 5, 6	Updated scope of the document. Updated list of reference documents Updated list of abbreviations. Updated results for GR740 silicon revision 1.
3.1	2018-11-20	1.2 6	Replaced obsolete document links. Updated text.
3.2	2018-11-27	1.2 4.1	Included reference to Dhrystone performance comparison results
3.3	2019-01-29	4.4.1 4.4.2	Included section title Added SpaceWire RMAP throughput results
3.4	2019-04-24	1.2 4.3 4.4.1 4.1	Included technical note title. Reframed sentence. Removed incorrect RMAP result. Corrected speedup value w.r.t. UT699

Issue	Date	Section / Page	Description
		6 4.1	Removed result description and added reference to ESCIES Radiation Summary Included ground rules

TABLE OF CONTENTS

1 INTRODUCTION

1.1 Scope of the Document

This document establishes the technical note on validation and benchmarking for the GR740 system-on-chip, developed within the European Space Agency Next Generation Microprocessor (NGMP) activities.

The work has been performed by Cobham Gaisler AB, Göteborg, Sweden.

Information and additional documentation for the GR740 device is available at the product webpage: http://www.gaisler.com/gr740

1.2 Reference Documents

[UMDS] "Quad Core LEON4 SPARC V8 Processor, GR740, Data Sheet and User's Manual", Cobham Gaisler, GR740-UM-DS version 2.0, July 2018
Online: http://www.gaisler.com/gr740

[GAIA] "RTEMS SMP Executive Summary, Development Environment for Future Leon Multi-core", RTEMSSMP-ES-001 issue 2 revision 2, March 2015 Online: http://microelectronics.esa.int/gr740/RTEMS-SMP-ExecSummary-CGAislerASD-OAR.pdf

[PPMSS] "Parallel Programming Models for Space Systems, Final Report", ppm4ss-FinalReport, June 2016 Online: http://microelectronics.esa.int/gr740/ppm4ss-FinalReport.pdf

[CMP] "Comparison between GR740, LEON4-N2X AND NGMP", GR740-CMP, Online: http://www.gaisler.com/doc/gr740/GR740-CMP.pdf

[SPW] Space engineering: SpaceWire - Links, nodes, routers and networks, ECSS-E-ST-50-12C, July 2008

[RMAP] Space engineering: SpaceWire - Remote memory access protocol, ECSS-E-ST-50-52C, February 2010

[SPWPNP] Space Engineering: SpaceWire Plug-and-Play protocol, ECSS-E-ST-50-54C, Draft, March 2013

[SPWD] SpaceWire-D - Deterministic Control and Data Delivery over SpaceWire Networks, Draft B, April 2010, ESA Contract Number 220774-07-NL/LvH

[BOUM] "GR-CPCI-GR740 Development Board User's Manual", Cobham Gaisler, GR- CPCI-GR740-UM, Version 1.7, January 2018.
Online: http://www.gaisler.com/gr-cpci-gr740

[CMARK] http://www.eembc.org/coremark/, 2016-09-09

[EEMBC] http://www.eembc.org/, 2016-09-09

[STTNS2013] "A 65nm CMOS platform for space applications: qualification test results on rad-hard microprocessors," P. Roche, G. Gasiot, S. Clerc, J. M. Daveau, C. Bottoni, M. Glorieux, V. Huard, and L. Dugoujon. IEEE Transaction on Nuclear Science, December 2013.

[GRLIB-TN-0015] "Dhrystone Performance: Compiler Versions and Ground Rules", https://www.gaisler.com/doc/antn/GRLIB-TN-0015.pdf

[ESCIES] https://escies.org/

[CG] http://www.gaisler.com/gr740

2 ABBREVIATIONS

AHB	Advanced High-performance Bus, part of AMBA 2.0 Specification
AMBA	Advanced Microcontroller Bus Architecture, bus architecture widely used for on-chip buses in SoC designs.
CPU	Central Processing Unit
DMA	Direct Memory Access
DSU	Debug Support Unit
FLOPS	Floating Point Operations Per Second
FPU	Floating Point Unit
I/O	Input/Output
KiB	Kibibyte, 2^{10} bytes, unit defined in IEEE 1541-2002
Mb, Mbit	Megabit, 10^6 bits
MB	Megabyte, 10^6 bytes
MiB	Mebibyte, 2^{20} bytes, unit defined in IEEE 1541-2002
MIPS	Million of Instructions Per Second
NGMP	Next Generation Microprocessor
OS	Operating System
PCI	Peripheral Component Interconnect
PROM	Programmable Read-Only Memory
RMAP	Remote Memory Access Protocol
SDRAM	Synchronous Dynamic Random Access Memory
SEL/SEU/SET	Single Event Latchup/Upset/Transient
SPARC	Scalable Processor ARChitecture
SOC, SoC	System-On-a-Chip
UART	Universal Asynchronous Receiver/Transmitter

3 OVERVIEW

The GR740 [UMDS] is a four LEON4FT core processor built around five AMBA AHB buses. One 128-bit Processor AHB bus, one 128-bit Memory AHB bus, two 32-bit I/O AHB buses and one 32-bit Debug AHB bus. The Processor AHB connects the four LEON4FT processor cores to a shared 2 MiB L2 cache. The Memory AHB bus is located between the L2 cache and the main external memory interface (SDRAM) and attaches a memory scrubber. The two separate I/O AHB buses connect peripheral cores such as PCI master/target, PROM/IO memory controller, timers, interrupt controllers, UARTs, general purpose I/O port, SPI controller, MIL-STD-1553B interface, Ethernet MACs, CAN controllers, and a SpaceWire router. The fifth bus, a dedicated 32-bit Debug AHB bus, connects a debug support unit (DSU), that allows for non-intrusive debugging through the DSU and direct access to the complete system.

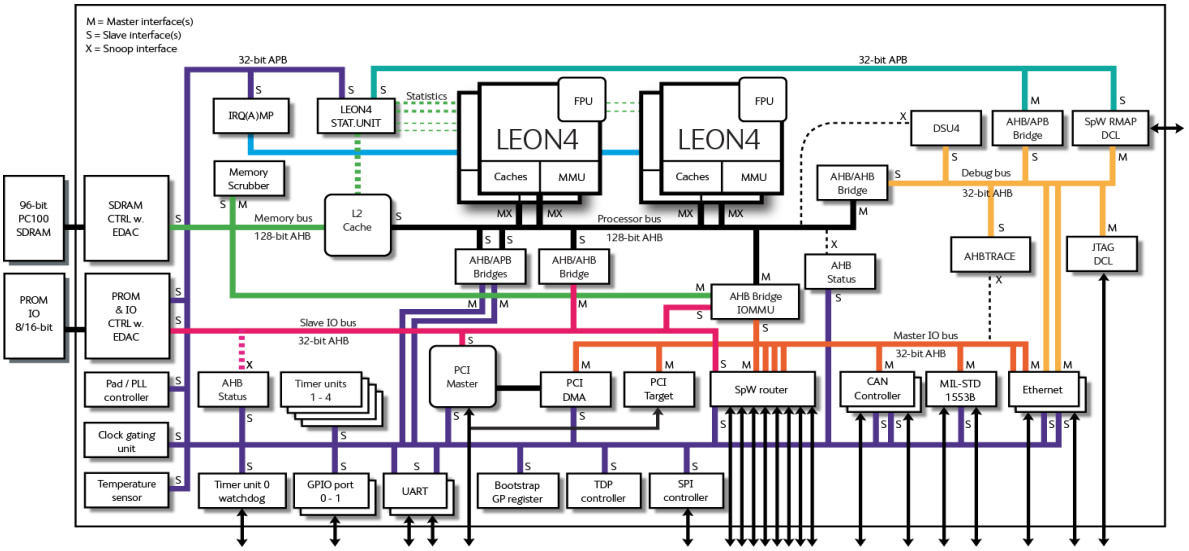


Figure 1. GR740 architecture block diagram

Following the manufacturing of the GR740 device an extensive test and validation effort has been undertaken. This technical note presents results from primarily the functional validation effort that was conducted using the GR-CPCI-GR740 [BOUM] development board (see figure 2).

More information, including user manuals for both the device and development board, can be found at the web pages:

- http://www.gaisler.com/gr740 – GR740 product page
- http://www.gaisler.com/gr-cpci-gr740 – GR-CPCI-GR740 product page

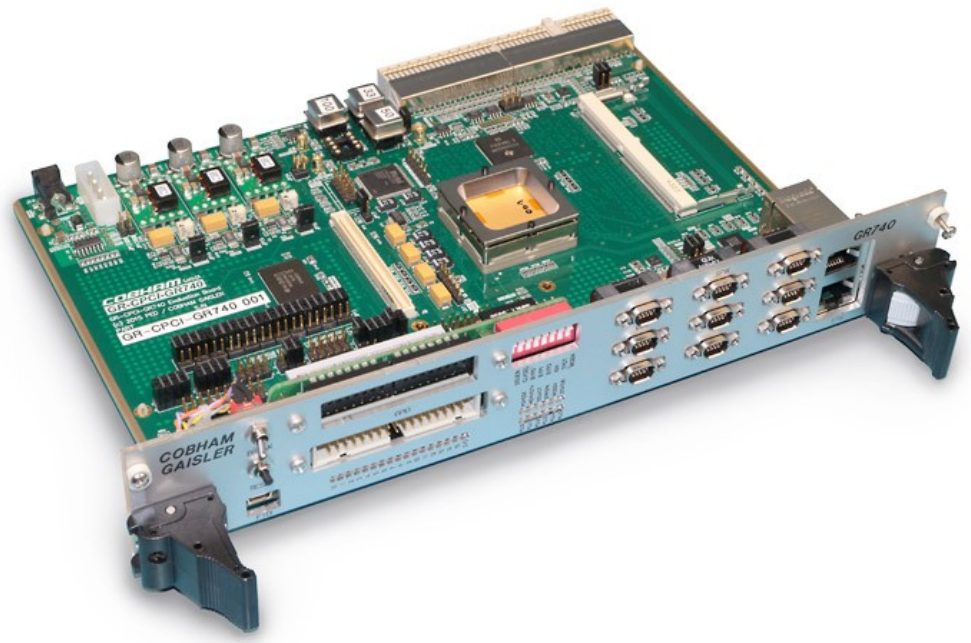


Figure 2. GR-CPCI-GR740 Development board

In addition to the benchmarking efforts performed by Cobham Gaisler there are also other evaluations that are applicable to the GR740 device. These include:

- RTEMS Multi-Core and GAIA VPU demonstrator [GAIA] – Comparison of PowerPC SCS750 and the LEON4-N2X device, which is a functional prototype of the GR740.
- Parallel Programming Models for Space Systems [PPMSS] - Evaluated the potential benefits of using the OpenMP tasking model into the space domain in terms of programmability, performance and time predictability.

Note that the GR740 device is the first rad-hard silicon that comes from the development done within the European Space Agency's Next Generation Microprocessor (NGMP) activities. During the development, several prototypes have existed and benchmark results and evaluation have been performed for these prototypes. The NGMP is an architecture that has evolved and changed over time, benchmark results obtained on prototypes may not be representative of the architecture finally implemented as the GR740. A comparison document between what was the final specification within the NGMP phase 1 activities, the functional prototype implementation (LEON4-N2X) and the first rad-hard silicon (GR740) is available in [CMP].

4 PROCESSING PERFORMANCE

4.1 Single core performance

Each LEON4FT is a SPARC V8 processor core with 7-stage pipeline, 8 register windows, 4x4 KiB instruction and 4x4 KiB data caches., MMU and a double-precision IEEE-754 FPU floating-point unit. The processor runs at 250 MHz nominal frequency, capable of executing one double precision FLOP per cycle per core. Several benchmark suites have been run on the processor:

- Each processor provides 459 Dhrystone MIPS (or DMIPS) per core , which gives 1.84 DMIPS/MHz.
- Each processor provides 200.6 Whetstone MIPS (or MWIPS), which gives 0.8 MWIP/MHz.
- The Linpack benchmark reports 22.7 MFLOPS.
- The EEMBC CoreMark reports : CoreMark 1.0 : 511.69 / GCC4.4.2 -O3 -mv8 -msoft-float -funroll-loops -fgcse-sm -combine -DPERFORMANCE_RUN=1 -mcpu=v8 -msoft-float / Stack [CMARK].
- The EEMBC Autobench 1.1 reports 113.53 AutoMarks[1] [EEMBC].
- The EEMBC FPMark 1.3.2470 reports 198.93 FPMarks[2] [EEMBC].
- The EEMBC CoreMark-Pro reports : CoreMark-PRO 1.1.2470: 84.86/ GCC 4.4.2 -g -O2 -mcpu=leon3 -std=c99 [EEMBC].

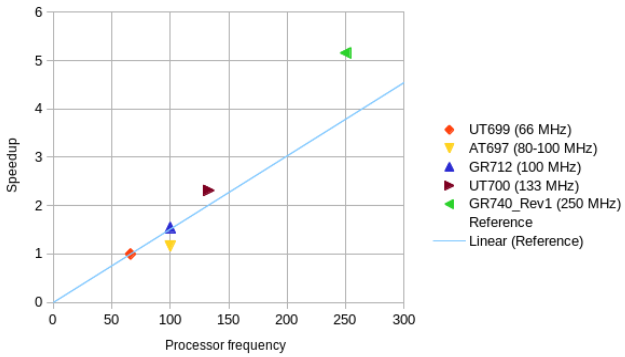


Figure 3. Cobham Gaisler device comparison (single-core)

1 Compiler version for Autobench: GCC 4.4.2

2 Compiler version for FPMark: GCC 4.4.2

Compared with previous generations of Cobham Gaisler devices, the GR740 provides a significant performance improvement, 5.16x with respect to the UT699, 3.33x with the GR712 and 2.23x with the UT700, as seen in the figure above. The speedup is obtained as an average improvement of a collection of benchmark figures, such as Dhrystone, Whetstone, Linpack, SPEC CPU2000 and other software applications. Please note that this result is single-core performance, which means that only one of the two cores of the GR712 and one of the four cores of the GR740 are used.

A comparison of performance using Dhrystone benchmark, compiled with different compiler versions, is available. Following ground rules were defined and followed during the comparison.

- Separate compilation
- No procedure merging (no inlining)
- Other optimizations are allowed, but they should be indicated
- Default results are those without "register" declarations (C version)

Please refer technical note [GRLIB-TN-0015] for more details.

4.2 Multi core performance

The GR740 comprises four LEON4FT that can theoretically provide 4 times the single-core performance. To evaluate the multicore performance we use PARSEC 3.0 benchmarks running on top of Linux OS. PARSEC are multithreaded benchmarks, representative of shared-memory programs for multiprocessors. These benchmarks are able to obtain 3.8x which is almost the maximum theoretical speedup in a four core processor (4x).

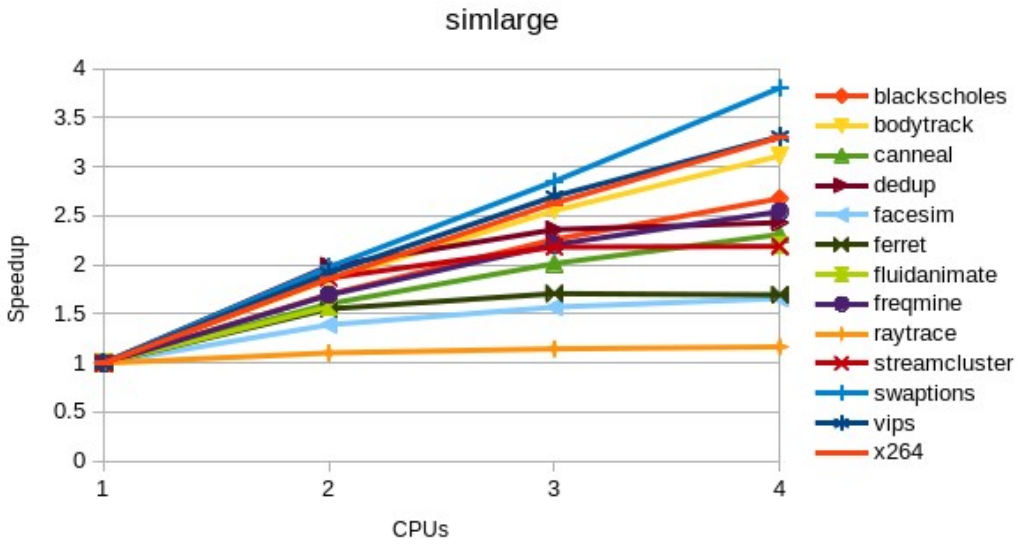


Figure 4. PARSEC 3.0 results.

Coremark-pro was executed with multi core support and achieved : CoreMark-PRO 1.1.2470: 232.05/GCC 4.4.2 -g -O2 -mcpu=leon3 -std=c99/4. We also used the EEMBC Multibench[3] 1.1 on top of Linux OS, reporting 69.3 MultiMark, 69.3 ParallelMark and 44.4 MixMark [EEMBC].

4.3 Impact of bus interference between processors

The GR740 uses a AMBA AHB bus to connect the four LEON4FT cores to the shared 2 MiB L2 cache. When more than one core try to access the L2 cache at the same time, only one of the cores gets access to the bus and the others have to wait. This interference translates into an increase of the overall execution time of the task running on the processor.

In order to mitigate this interference, the GR740 implements an AHB bus with split transactions, which means that when a core accessing the bus is waiting for a response (such a L2 cache miss that has to go to fetch data from memory), another core can use the bus while that response becomes available. This greatly reduces the impact of bus interference and reduces the bottlenecks of parallel execution.

To illustrate the impact of split transactions, we have devised an experiment based on two microkernels: one designed to suffer the worst possible impact of interference on the bus (a.k.a. victim) and another one that generates the worst interference possible on the bus (a.k.a. interferer).

3 Compiler version for Multibench: GCC4.9

We run one victim in one of the cores against 1, 2 or 3 interferers on the other cores and measure the victim's increase on execution time. The following figure clearly shows how the split transactions reduce the impact of interference, up to 3.35x times less interference in the worst-case.

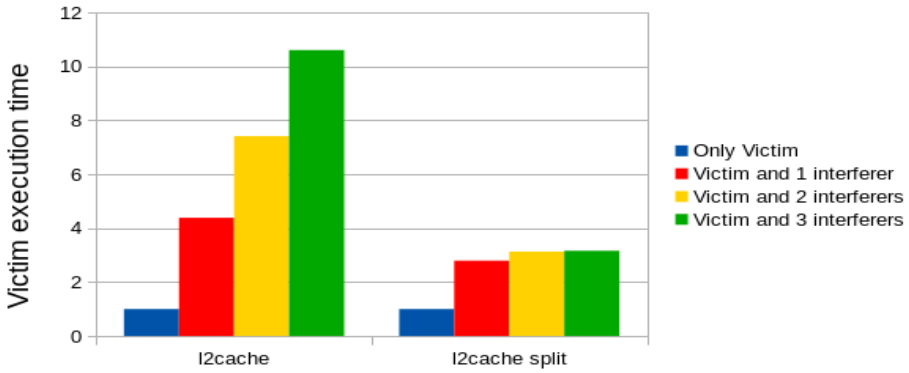


Figure 5. Impact of AMBA SPLIT transactions on bus interference

Please note that this level of interference is very unlikely to happen in real life, since these microkernels are constantly and solely using the bus (therefore constantly missing on the L1 caches). Typical software will spend most time executing from private L1 caches.

4.4 I/O performance

4.4.1 Overview

The GR740 has a SpaceWire router with eight SpaceWire links . The router implements a routing switch, as defined in [SPW] with a RMAP target for configuration [RMAP]. Among the features supported by the router are: group adaptive routing, packet distribution, system time-distribution, distributed interrupts, port timers to recover from deadlock situations, SpaceWire-D [SPWD] packet truncation based time-slot violations, and SpaceWire Plug-and-Play [SPWPNP]. Each SpaceWire link can operate at 400 MHz, providing an effective measured data transfer rate of 320 Mbps. A detailed analysis results for RMAP performance is available at section 4.4.2.

The GR740 also has a 32 bit PCI Initiator/Target interface with DMA that can achieve data transfer rates of 831.3 Mbps with a 33 MHz PCI clock.

The device also includes 2x 10/100/1000 Mbit Ethernet, MIL-STD-1553B interface, 2x CAN 2.0 controller interface and SPI.

The validation effort has been performed both on engineering models (silicon revision 0) and for the silicon revision used for flight models (silicon revision 1).

4.4.2 SpaceWire RMAP performance

SpaceWire RMAP performance analysis was performed with GR-CPCI-GR740 board, both as initiator and target. SpaceWire cables were connected between SpaceWire port 1,2,3 and 4 of initiator and corresponding ports of target. Throughput was measured, with SpaceWire traffic only on single link and also with SpaceWire traffic on four links running at the same time. To calculate write and read rate, two types of transmissions were performed. Transmission of one packet at a time and multiple packets transmitted as a burst.

The test was performed with run state link rate for both initiator and target configured as 200Mbps. The following tables contains test results for packet size 1MiB.

ID	Number of links	RMAP packet size (bytes)	Total RMAP data bytes sent	Number of packets	SpaceWire clock frequency (MHz)	SpaceWire link rate (Mbps)	One packet at a time		Packets as a burst	
							Write rate (Mbps)	Read rate (Mbps)	Write rate (Mbps)	Read rate (Mbps)
1	Single link	1048544	4194176	4	400	200	159.88	159.91	159.92	159.94

Table 1: SpaceWire RMAP throughput with traffic on single link

ID	Number of links	RMAP packet size (bytes)	Total RMAP data bytes sent	Number of packets	SpaceWire clock frequency (MHz)	SpaceWire link rate(Mbps)	One packet at a time			
							Write rate Four links combined (Mbps)	Write rate Per link (Mbps)	Read rate Four links combined (Mbps)	Read rate Per link (Mbps)
1	Four links	1048544	16776704	16	400	200	635.9	158.97	636.31	159.07

Table 2: SpaceWire RMAP throughput with traffic on four links – One packet at a time

ID	Number of links	RMAP packet size (bytes)	Total RMAP data bytes sent	Number of packets	SpaceWire clock frequency (MHz)	SpaceWire link rate(Mbps)	Packets as a burst			
							Write rate Four links combined (Mbps)	Write rate Per link (Mbps)	Read rate Four links combined (Mbps)	Read rate Per link (Mbps)
2	Four links	1048544	16776704	16	400	200	636.41	159.1	636.5	159.12

Table 3: SpaceWire RMAP throughput with traffic on four links – Packet burst transmission

As part of characterization, packets with size 1KiB, 2KiB and 4KiB were also used for transmission. For smaller packets, observed throughput was low since the CPU over head for packet handling is comparatively high. Reported throughput is considered representative when packet size is 1MiB since it triggers L2 cache misses and there by exercises external SDRAM.

5 POWER CONSUMPTION

Several power measurements have been carried out with the processor on the default configuration (processor at 250 MHz and memory at 100 MHz) and running at 50 MHz. The measurements are taken reading the available power measurement circuits on the board (via I2C) at room temperature. These measurements provide Voltage and Current of the three device supply lanes: i) 1V2 – Core supply, ii) 2V5 – IO LVDS supply and iii) 3V3 – IO supply. These values are sampled every second and the mean power consumption over time is computed on each scenario.

The different scenarios comprise the processor at reset (1), idle (2), or running different benchmarks. The Dhrystone and Coremark single-core benchmarks with LVDS signals on and off are used in scenarios 3, 4, 5 and 6. A PARSEC benchmark is run using one and four cpus in scenarios 7 and 8. The SPEC CPU2000 benchmarks are run also with one and four cpus in scenarios 9, 10, 11 and 12. All scenarios use the nominal frequency, 250 MHz, except 11 and 12 that run at 50 MHz.

Please note that no internal clock is present during the reset scenario (scenario 1) since while asserting reset the PLLs are held in power down and no clock goes into the system. Also note that the LVDS SpaceWire signals can be turned off to reduce its power consumption (roughly 200 mW).

The next scenarios, from 13 to 16, use a single-core RTEMS application to transfer data using SpaceWire at different link speeds or internally on the Spacewire router. The last scenarios, 17 and 18, run the ttcp application on top of Linux SMP using all four cpus (17) and RTEMS single-core (18). Table 4 and Figure 6 summarize results, showing the power consumption for different supplies and the total power consumed (addition of all three supply lanes):

Scenario	Description	Core Power	LVDS Power	I/O Power	Total Power
1	Processor hold at reset	42	345	166	553
2	Idle (LVDS on)	316	350	248	914
3	Dhrystone (LVDS off)	506	159	249	914
4	Dhrystone (LVDS on)	528	350	250	1128
5	Coremark (LVDS off)	523	149	254	926
6	Coremark (LVDS on)	525	350	251	1127
7	PARSEC (single core/LVDS off)	532	145	251	928
8	PARSEC (all cores/LVDS off)	1010	145	235	1391
9	CPU2000 (single core/LVDS on)	645	380	189	1213
10	CPU2000 (all cores/LVDS on)	1161	371	272	1804
11	CPU2000 (single core/LVDS on) @ 50 MHz	157	378	111	645
12	CPU2000 (all cores/LVDS on) @ 50 MHz	292	378	95	765
13	Spacewire router internal traffic (LVDS on)	620	420	268	1308
14	Spacewire 100 MHz link-rate (LVDS on)	593	429	228	1250
15	Spacewire 200 MHz link-rate (LVDS on)	603	433	273	1309
16	Spacewire 400 MHz link-rate (LVDS on)	626	449	278	1353
17	Ethernet Linux SMP (all cores/LVDS on)	1036	373	241	1649
18	Ethernet RTEMS UP (single core/LVDS on)	420	350	247	1017

Table 4: Power measurements in mW (GR740 revision 0)

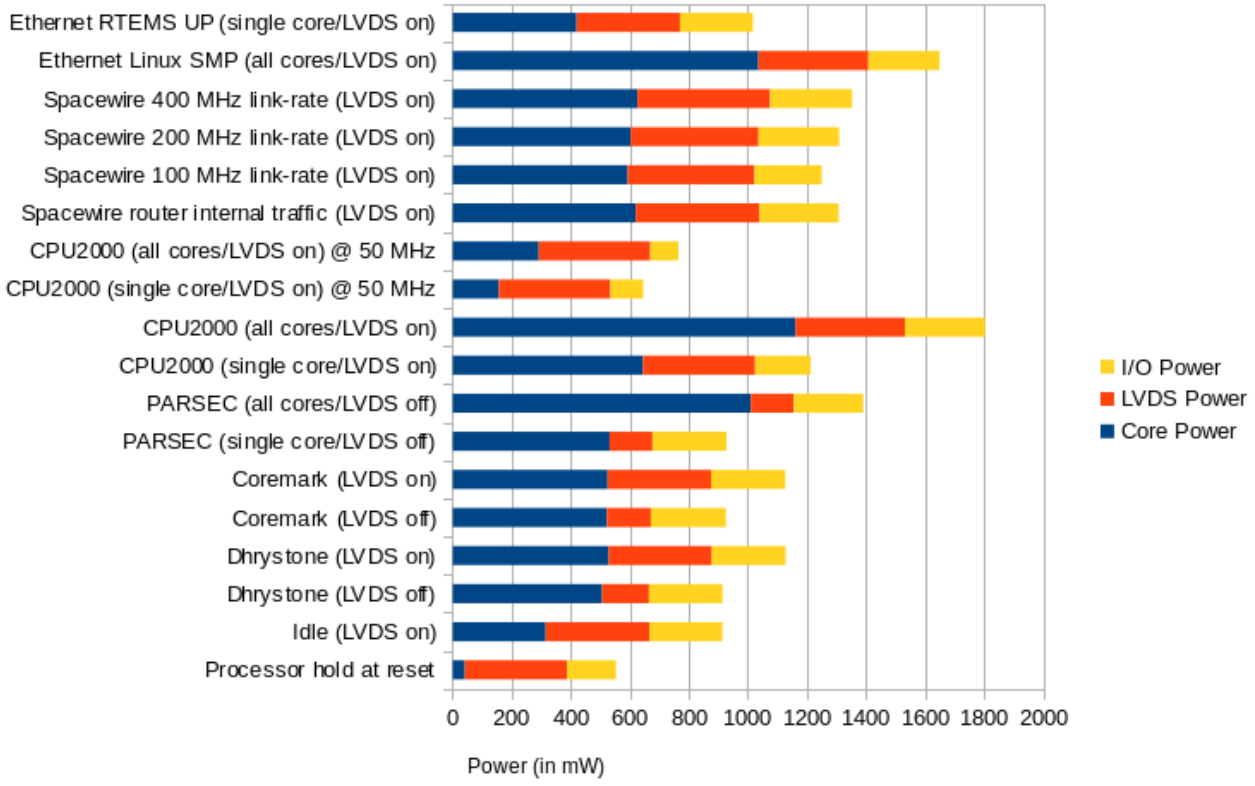


Figure 6: Power measurements in different scenarios (GR740 revision 0)

The average power consumption for core, LVDS and I/O power for revision 1 GR740 is listed in the table below.

Scenario	Description	Core Power-Rev1(mW)	Core Power-Rev0(mW)	LVDS Power-Rev1(mW)	LVDS Power-Rev0(mW)	I/O Power-Rev1(mW)	I/O Power-Rev0(mW)
9	CPU2000 (single core/LVDS on)@250 MHz	605.09	645.00	440.58	380.00	185.29	189.00
10	CPU2000 (all cores/LVDS on)@250 MHz	1,189.72	1,161.00	439.23	371.00	285.82	272.00

Table 5: Power measurements in mW for GR740 revision1

6 RADIATION TOLERANCE

A Radiation Summary presenting the radiation performance of GR740 flight silicon will be published online on the ESCIES's website [ESCIES] and Cobham Gaisler website [CG].